Advances in Silicon Technology Enables Replacement of Quartz-Based Oscillators

I. Introduction

With a market size estimated at more than $650M and more than 1.4B crystal oscillators supplied annually[1], quartz crystal oscillators have long been the preferred choice for clock generation in consumer, computing, and communication applications. Quartz oscillators are available in a wide range of frequencies, package sizes, and stabilities. In addition to providing excellent jitter performance, quartz oscillators are available from a broad range of suppliers. Yet for all their benefits, manufacturing complexity and reliability issues associated with quartz oscillators have driven the quest to develop alternative oscillator solutions that use micro electromechanical (MEMs) resonators or pure semiconductor solutions like the Si500.

II.a. Quartz Resonator Based Oscillators

Crystal oscillators require a unique quartz resonator for each frequency. The crystal oscillator assembly process requires the quartz to be cut, x-rayed, lapped, mounted, and sealed into the final package (Figure 1). Fabrication of these resonators becomes increasingly difficult at frequencies over 100 MHz because the resonator must be manufactured to very tight tolerances. The complexity of the manufacturing process is subject to poor yield at multiple steps within the process forcing material restarts and overall production delays. This built-to-order process flow makes it difficult for oscillator suppliers to implement statistical quality control or continuous improvement because every oscillator frequency must be managed as a separate product. The end result is long unpredictable lead times, especially for custom frequencies that the manufacturer has not made in high volume.

In addition to lead times, reliability is a chief concern with quartz oscillators. Quartz oscillators are susceptible to contamination which can affect both the center frequency and the ability of the XO to start up reliably. If an oscillator fails in the end application, often the entire system fails because the oscillator provides critical timing for the electronics.

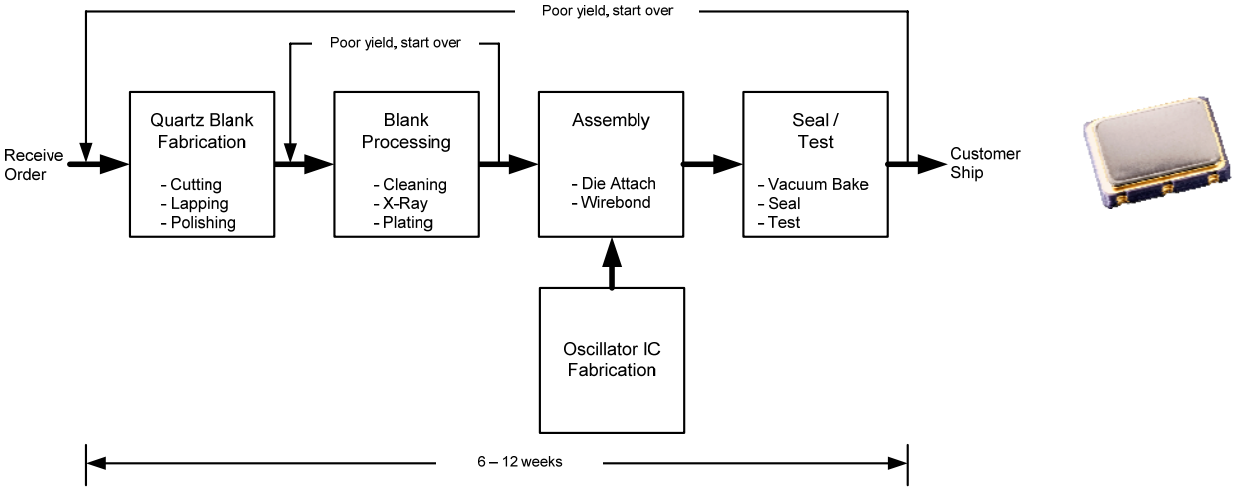

Figure 1 — Quartz Oscillator Manufacturing Flow

II.b MEMS Resonator Based Oscillators

The industry has long been searching for a technology that enables the replacement of quartz oscillators with a solution that addresses lead time and reliability concerns while providing performance on par with quartz oscillators. Over the last several years, micro-electromechanical system (MEMS)-based oscillators have emerged as a possible replacement technology for quartz oscillators. MEMS-based oscillators provide an alternative solution to quartz by replacing the quartz oscillator with a CMOS-based mechanical resonator. While MEMS oscillators have been adopted in some <125 MHz frequency applications, they have been challenged to provide a comparable solution to quartz in terms of jitter and phase noise performance. In addition, MEMS oscillators have traditionally been limited to a narrow frequency range and have not been constructed to support the wide range of signal formats required by the electronics industry. Finally, MEMs oscillators require specialty wafer processing techniques for the MEMs resonator that complicate the oscillator assembly process.

The MEMs oscillator is constructed by combining a silicon resonator fabricated using MEMs techniques with a phase-locked loop IC capable of synthesizing different output frequencies (see Figure 2). This approach has the advantage of using a common resonant structure and common PLL IC to generate a wide range of different frequencies. While the MEMs resonator is fabricated using standard semiconductor processing techniques, the resonator must be hermetically sealed using more complicated wafer bonding techniques. Once fabricated, the MEMs resonator can then be assembled with the PLL IC into a finished product that is tested and programmed to a customer's specific frequency. The manufacturing flow for MEMs oscillators is an improvement over traditional crystal oscillators but it relies on non-standard semiconductor wafer processing techniques that are not widely available across the industry. As a result, manufacturing options are reduced and business continuity planning is complicated.

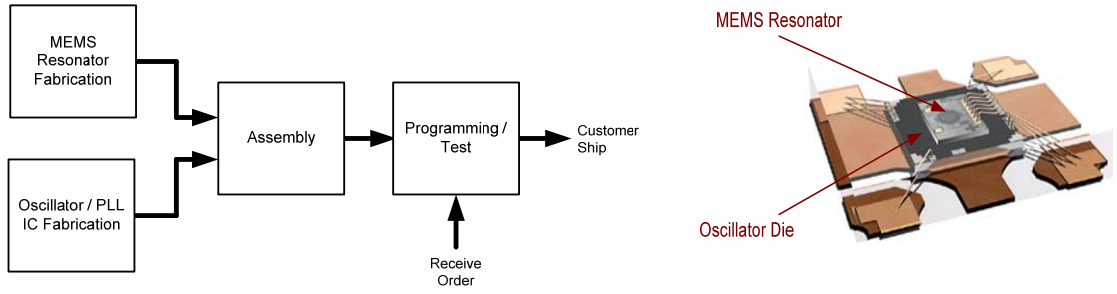

Figure 2 — MEMS Oscillator Manufacturing Flow

II.c Si500 Silicon Oscillator

Silicon Lab's Si500 silicon oscillator leverages a standard IC manufacturing flow (Figure 3). The silicon oscillator is fabricated using standard submicron CMOS technology and standard low-cost plastic packaging that does not require a hermetic seal. The silicon oscillator is factory-programmed at test to a specific frequency, signal format, and supply voltage. A single un-programmed silicon oscillator can be used to generate any frequency from 0.9 to 200 MHz, enabling quick turn delivery of standard and custom frequency oscillators (2 weeks or better). Every Si500 oscillator leverages an identical, low cost standard IC manufacturing flow, enabling economies of scale while providing comprehensive quality monitoring and statistical process control.

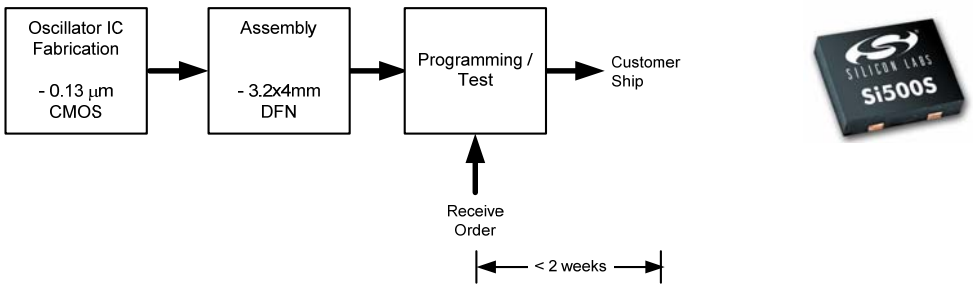

Figure 3 — Silicon Oscillator Manufacturing Flow

III. Si500 Technology Overview

Figure 4 provides a block diagram of the Silicon Labs Si500 silicon oscillator. The heart of the architecture is a low phase noise, frequency flexible LC oscillator. Using innovative mixed-signal analog circuitry, the oscillator is compensated for frequency variation due to operating temperature range, aging, initial frequency accuracy, supply voltage change, and output load change. The silicon oscillator supports a wide frequency range, generating any output clock frequency from 0.9 to 200 MHz. Selection of the frequency, output type, supply voltage, and output enable (OE) is stored in non-volatile memory (NVM). At power-on, the Si500 performs a self-calibration using these stored parameters and configures itself for operation.

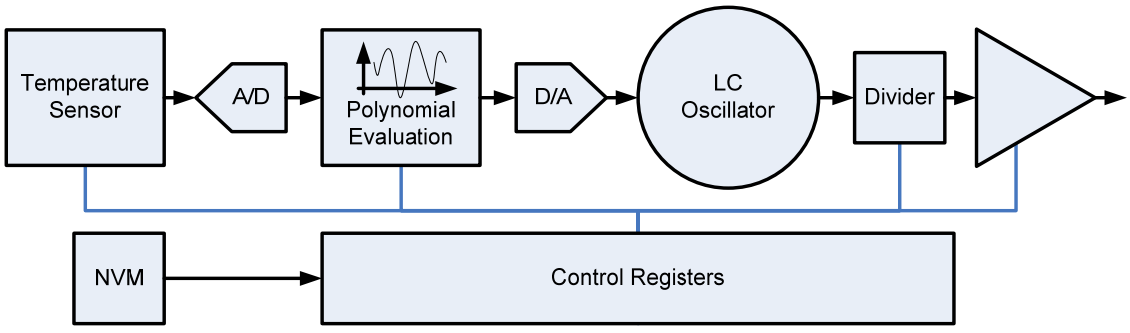

Figure 4 — Si500 Silicon Oscillator Block Diagram

IV. Temperature Stability

Temperature stability refers to how much the oscillator frequency varies over the operating temperature range of the device. For the Si500 silicon oscillator, tight temperature stability is achieved through dynamic temperature compensation. The device has an on-board temperature sensor that, upon detection of a temperature change, dynamically adjusts the frequency of oscillation of the LC oscillator to maintain a stable output frequency. Temperature compensation is performed by digitizing the temperature sensor output and adjusting the center frequency of the LC oscillator. The temperature response of the internal oscillator is calibrated for each device as part of the outgoing test procedure. By individually compensating each device, device to device variation is minimized. The Si500 uses a multi-order polynomial fit to meet ±10 ppm (typical) temperature stability, delivering performance comparable to quartz oscillators. Figure 5 compares the temperature stability of the Si500 with competitive quartz and MEMS-based oscillators.

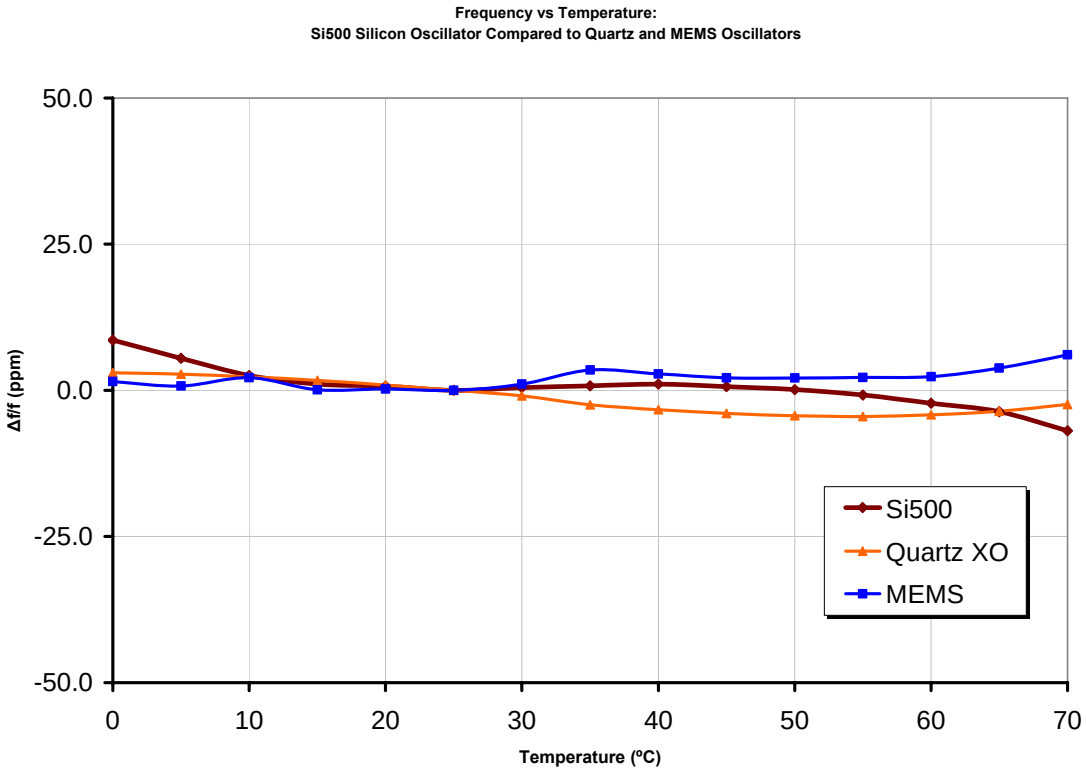

Figure 5 —Temperature Stability Comparison

V. Aging

All oscillators experience drift in the frequency over long periods of time. The effect is called "aging" and is an important specification in the overall frequency stability budget. Aging behavior is dependent on several aging mechanisms including the design of the resonator, the assembly of the oscillator, the contamination level surrounding the resonator, the design of the electronics, and the operating temperature. To determine an upper bound on aging performance, it is necessary to control as many of the mechanisms as possible and to verify conformance through extensive aging studies. Because the Si500 resonator is constructed with adjacent layers of

material, contamination cannot affect its frequency. Instead, the Si500 frequency aging behaves like other semiconductor aging mechanisms.

Semiconductor aging mechanisms are well understood and often follow the Arrhenius equation for reaction rates. The Si500 frequency aging demonstrates an activation energy of ~0.7 eV, which matches other common semiconductor reaction rates. Employing the Arrhenius equation, aging rates can then be estimated for various operating temperatures from higher temperature qualification data. Figure 6 shows the mean aging for common operating temperatures over time extrapolated from data collected at 125 °C.

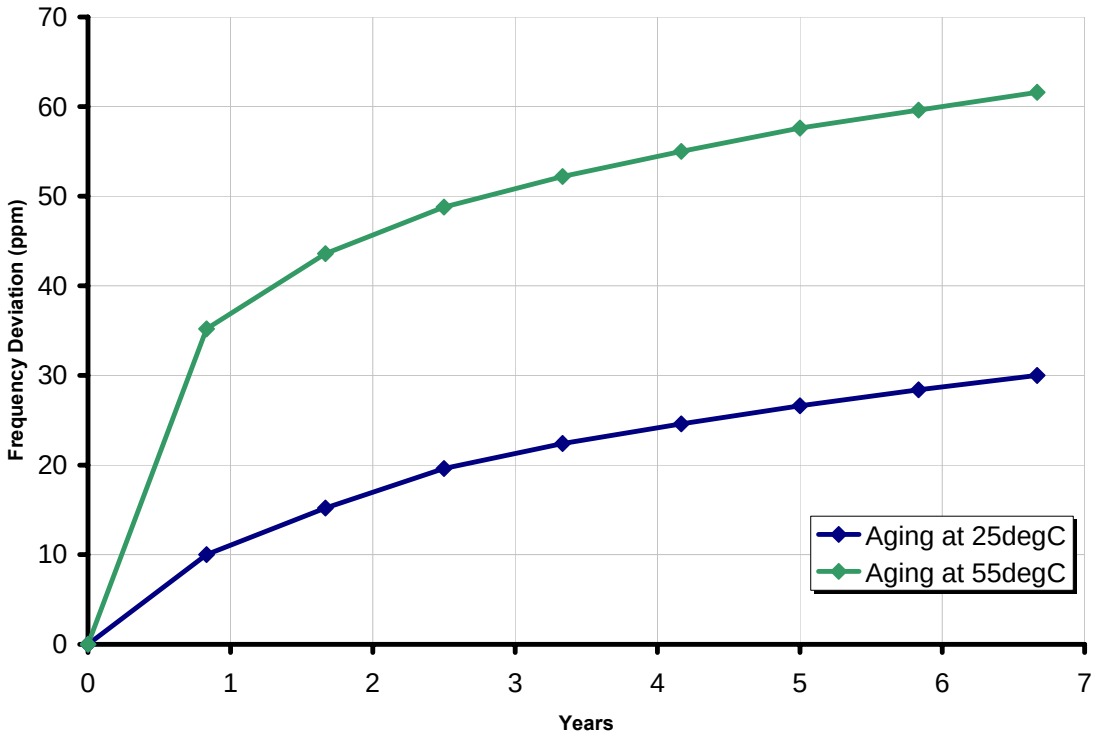

Figure 6—Estimated Aging for Si500 Silicon Oscillator at 25 and 55 °C

VI. Reliability

Quartz oscillators require hermetic packaging for the crystal. Package leaks or internal contamination can lead to long term frequency aging, or if severe enough, can even prevent oscillation. Consequently, oscillator manufacturers minimize contamination by using costly, hermetically sealed ceramic or metal packaging and special processing. Done properly, reliable operation can be achieved, but package and assembly costs will be considerably higher than with non-quartz CMOS only devices. Being a mechanical device, MEMS resonators are susceptible to the same contamination issues and also require hermeticity. While hermeticity can be achieved using wafer level processes for MEMS resonators, they are very specialized and also add cost.

In contrast, the Si500 relies on standard, high-volume CMOS IC manufacturing and low cost plastic packaging. Since the Si500 has no moving parts and does not require hermetic assembly, it is not susceptible to contamination related frequency shifts and possible loss of signal. The Si500 has a more robust start-up because loss mechanisms are dominated by metallic resistances associated with metal wiring, which are very constant over time, thereby making the oscillation margin nearly constant over time. In addition, test circuitry within the Si500 allows

Silicon Labs to effectively screen for oscillator margin as part of the outgoing test procedure, ensuring each device has sufficient oscillation margin over the lifetime of the product.

VII. Shock and Vibration

Shock and vibration can also limit the reliability of quartz-based oscillators. Quartz crystals are mounted above the oscillation electronics using epoxy or metal clips supported on one side only (Figure 7). Attaching the crystal on one side places the crystal's center of gravity far away from the support point allowing the crystal to swing like a diving board when exposed to vibration. Large shock events can crack the crystal, and continued vibration can damage the crystal attachment. Instead of mechanical structures, the Si500 uses an all-electronic oscillator with no moving parts thereby maintaining a single center of gravity. Since the Si500 does not rely on a mechanical resonator for oscillation, oscillation is very robust in high shock and vibration environments.

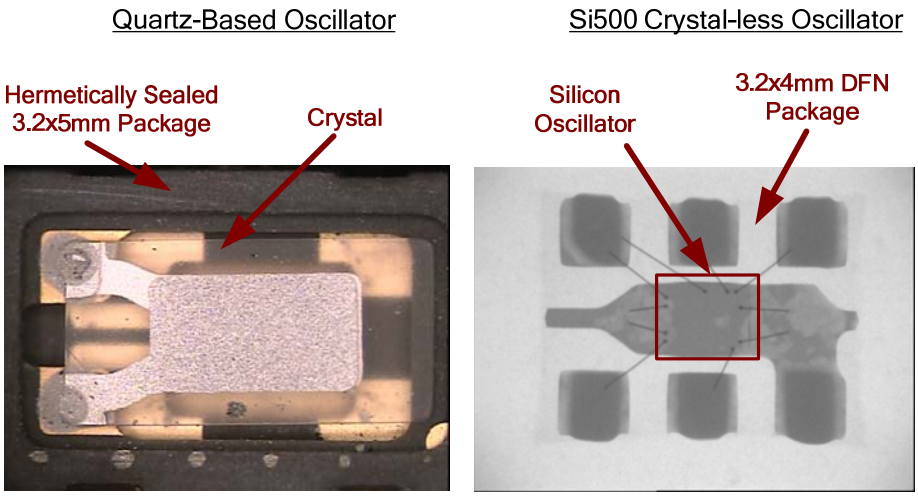

Figure 7 — Si500 vs. Quartz XO Packaging Comparison

VIII. Jitter Performance

Period jitter is a key specification for oscillators since it impacts the setup/hold time, noise margin, or bit-error rate of systems that require alignment between clock and data. Period jitter describes how much any period may deviate from the ideal clock period and is used to determine the setup/hold time margin within a digital system. The amount of margin required depends greatly on the how many timing violations (i.e., bit-errors) a system can handle. In most designs, no timing violations are allowed over the lifetime of the product, so the amount of margin is quite large.

Period jitter is related to phase noise[2] and is often dominated by phase noise at far offset frequencies up to half of the clock frequency. At far offsets, the performance of the output buffer dominates the phase noise and is independent of the oscillator Q (quality factor). For this reason, a low noise output stage is required to achieve good period jitter performance.

The Si500 output buffer was specifically designed to provide very low noise and high rejection to power supply interference. The impact of the design quality can be seen in the period jitter comparison in Table 1 and is a direct result of the PSRR shown in Figure 8. The Si500 provides

period jitter performance that is better than quartz oscillators and significantly better than MEMS oscillators.

Device	Period Jitter (typ)
Si500 silicon oscillator	0.8 ps
EG2101CA quartz oscillator	1.0 ps
FXO HC735 quartz oscillator	1.3 ps
CPPLC5 LT06T quartz oscillator	2.0 ps
EMK23H2H MEMS oscillator	6.0 ps

Note: devices measured at 100 MHz

Table 1 — Jitter Performance Comparison

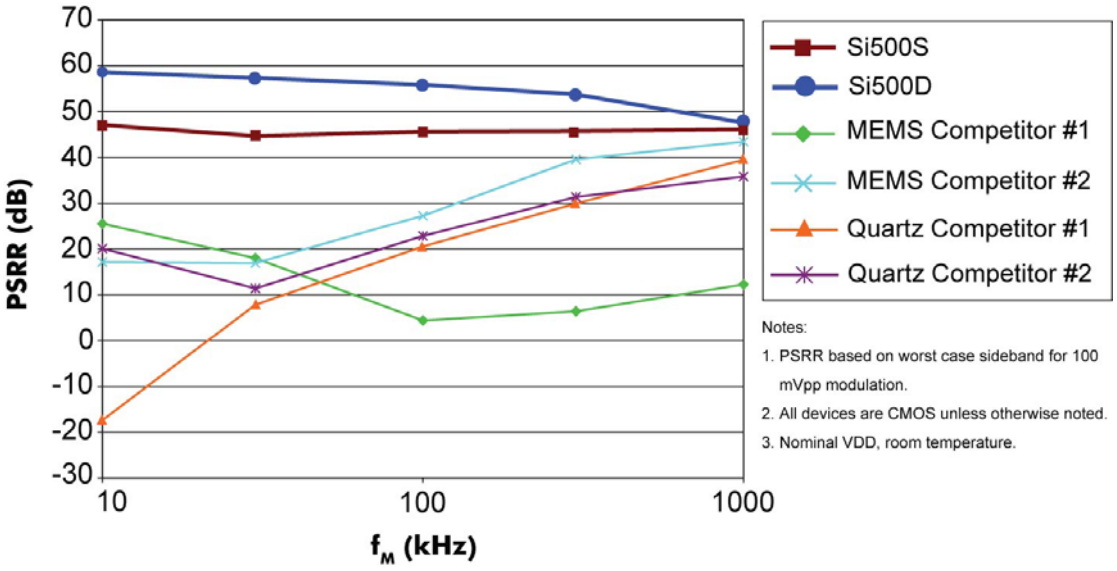

Figure 8 — PSRR Comparison

IX. Programmable Output Buffer

Because the Si500 can generate frequencies across a large range (0.9 to 200 MHz), the output buffer design must provide easy connectivity for the many common receiver formats and voltages used in this range. The Si500 employs a programmable output buffer with support for both differential and single-ended formats (see Table 2) while easing the design effort by incorporating common external components. Existing oscillator solutions have traditionally supported either CMOS for lower frequencies (<150 MHz) or LVPECL for higher frequencies (40 to 200 MHz). By supporting a wider range of formats and voltages natively, the Si500 eliminates the need for external buffers and level translators. As systems increase density, differential signal formats provide better immunity to interference, which translates into better jitter performance. The Si500 utilizes a flexible programmable buffer that supports the LVPECL standard as well as newer standards such as LVDS (common on ASICs and FPGAs) and HCSL (for PCI Express). The differential formats are available for any output frequency easing the density concerns regardless of application. In addition, the Si500 can be ordered with the output buffer configured to provide two CMOS outputs that are either in-phase or out of phase by 180°. By supporting a wide range of output types, the Si500 easily addresses the connectivity and signal integrity needs for applications from 0.9 to 200 MHz.

Si500 Output Formats	Si500 Output Voltages
CMOS (singled-ended, dual output, or differential)	3.3 V, 2.5 V, 1.8 V
LVDS	3.3 V, 2.5 V, 1.8 V
LVPECL	3.3 V, 2.5 V
Low power LVPECL	3.3 V, 2.5 V
HCSL	3.3 V, 2.5 V, 1.8 V
SSTL-3, SSTL-2, SSTL-18	3.3V, 2.5 V, 1.8 V

Table 2 — Si500 Output Format and Output Voltage Options

X. Conclusion

With advances in mixed-signal CMOS technologies, silicon oscillators like the Si500 are now competitive with oscillators that use traditional quartz or MEMS resonators. By eliminating the need for these mechanical resonators, the Si500 offers significantly improved reliability when shock, vibration, and oscillator start up are considered. In addition, the Si500's simplified manufacturing flow reduces cost and enables short predictable lead times when compared to traditional quartz based oscillators. Compared to other <200 MHz oscillators, the Si500 provides improved jitter performance, a wider range of output format options, and significantly better supply noise rejection.

References:

[1] Frequency Control Components – Global Markets, Applications, and Competitors: 2007 – 2012 Analysis & Forecasts, Dedalus Consulting, 2008.

[2] AN279: Estimating Period Jitter from Phase Noise, Silicon Labs, 2006.