Application with SCALE-2 Gate Driver Cores

Single and Dual-Channel SCALE-2 IGBT and MOSFET Driver Cores

Introduction and Overview

The SCALE-2 IGBT and MOSFET gate driver cores are highly integrated low-cost components which provide the user with the highest level of technology and functionality for industrial and traction requirements. These features, coupled with their flexibility of design, have already made many power converters highly successful. Nevertheless, SCALE-2 gate driver cores are not plug-and-play gate drivers. A minimum understanding of power electronics is therefore necessary to develop reliable inverter systems with these cores.

This application note will highlight important design rules to help users and avoid qualification problems. Moreover it will help to speed up the development time by showing detailed examples about how to design SCALE-2 gate driver cores successfully.

Considered SCALE-2 gate driver cores are: 2SC0108T, 2SC0435T, 2SC0650P and 1SC2060P.

For applications with 2SD300C17, please contact support@IGBT-Driver.com

Fig. 1 SCALE-2 gate driver cores
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Applications with SCALE-2 Products

A successful use of SCALE-2 gate driver cores is coupled with an appropriate overall design. The key points listed below are success factors for the use of SCALE-2 gate drivers:

- Topology (e.g. how to parallelize IGBT modules)
- Schematics and right choice of components
- Geometrical location of IGBT gate drivers (where to place gate drivers)
- Magnetic field influences
- Clearance and creepage distances
- PCB layout
- Use of standards
- EMI considerations

SCALE-2 in Different Topologies

Use of SCALE-2 gate driver cores in three-level or multilevel topologies

During the operation of three-level converters, regular semiconductor commutation ensures that the inner IGBTs/MOSFETs are not turned off when the outer IGBTs/MOSFETs are in the on-state in order to avoid the full DC-link voltage being applied to the corresponding power semiconductors.

This situation must be considered when using CONCEPT SCALE-2 gate drivers. Such events could happen if the protection function of the gate drivers detects a short circuit or power-supply undervoltage. After fault detection, the gate driver turns the corresponding channel off immediately. The power semiconductors are not usually designed to withstand the full DC-link voltage. Destruction of the power semiconductor can consequently be prevented only if an adequate protection scheme is applied.

SCALE-2 Advanced Active Clamping protects the IGBT/MOSFET from excessive collector-emitter voltages in such situations. It therefore obviates the need to provide a dedicated turn-off sequence for the driver channels to be turned off in the fault condition - instead, the turn-off commands may be applied at any time within 3µs after fault feedback. It is recommended to apply a common turn-off command to all IGBT drivers within the converter to achieve a stable system state after fault feedback.

Please also refer to the application note AN-0901 /4/ on www.IGBT-Driver.com/go/app-note for more information.

Note: The under-voltage protection function of the SCALE-2 chipset cannot be disabled. The gate driver channel is turned off as soon as an under-voltage event is detected on the primary or secondary side. Use of active clamping consequently offers the best protection. In such cases, however, CONCEPT highly recommends testing the effectiveness of the active clamping function in the final converter design.
Use of a single SCALE-2 gate driver for paralleled IGBTs/MOSFETs

**Advanced Active Clamping in parallel IGBT operation with one common driver core**

Active clamping is a technique designed to partially turn on the power semiconductor as soon as the collector-emitter (drain-source) voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation.

Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor devices (TVS) to the IGBT gate. Most SCALE-2 products support CONCEPT’s Advanced Active Clamping, where feedback is also provided to the driver’s secondary side at pin ACLx: As soon as the voltage on the right side of the 20Ω resistor of Fig. 3 exceeds about 1.3V, the turn-off MOSFET is progressively switched off in order to improve the effectiveness of the active clamping and reduce the losses in the TVS. The turn-off MOSFET is completely switched off when the voltage on the right side of the 20Ω resistors approaches 20V (measured with respect to COMx). In parallel IGBT operation with the use of only one driver core, Advanced Active Clamping needs to control all parallel-connected IGBTs/MOSFETs. A separate feedback to every gate is required according to Fig. 3.
Fig. 3  Active clamping by paralleling three IGBTs/MOSFETs with one common gate driver core

It is recommended to use the circuit shown in Fig. 3 for parallel operation with one gate driver core. For dimensioning the TVS, Raclx, Caclx, D3x and D4x, please refer to the corresponding application manual. Note that at least one of the series connected TVS must be of bidirectional type.

\textbf{V \textsubscript{CE} sat in parallel operation with one driver core}

In general, CONCEPT recommends the use of only one \textit{V \textsubscript{CE} sat} detection circuit by using only one central gate driver core for paralleled IGBTs/MOSFETs, as this is sufficient to efficiently protect the system. The \textit{V \textsubscript{CE} sat} detection is connected to one of the parallel-connected IGBTs/MOSFETs. All paralleled IGBTs desaturate at the same time in the short-circuit condition. The maximum short-circuit current is limited by the IGBTs.

It is not recommended to connect auxiliary collectors of paralleled high-side IGBTs, as:

- A large offset current may flow and
- Oscillations may occur.

Moreover, the measurement of over-current via the \textit{V \textsubscript{CE} sat} detection is basically not recommended.

Fig. 4  \textit{V \textsubscript{CE} sat} detection by paralleling three IGBTs with one gate driver core

\textbf{Direct paralleling}

Parallel-connected IGBTs are conventionally driven by a common driver, with individual gate and emitter resistors for each IGBT (see last paragraph). An alternative approach to driving parallel-connected IGBT modules is to use an individual driver for each module (direct paralleling).

If direct paralleling of SCALE-2 drivers is required, please refer to the application note AN-0904 /5/ on www.IGBT-Driver.com/go/app-note
**Use of optical interface with SCALE-2 gate drivers**

For applications requiring optical PWM inputs and optical fault outputs, CONCEPT products permit different solutions. Beside standard plug-and-play driver solutions for high-voltage IGBTs, an alternative solution is to just use an optical interface in front of a SCALE-2 IGBT gate driver core. Figure 5 shows an example of how to drive a SCALE-2 driver core with a standard Avago HFBR type. A Schmitt-trigger CD40106 inverts the output signal of the HFBR-2522 into a 5V logic signal. This signal drives the SCALE-2 gate driver core. The open drain fault outputs SO1 and SO2 have a 1kΩ pull-up resistor to drive the optical interface. The light is on during the normal condition and is off in the fault condition. The diode current during normal operation is about 15mA. During the fault condition, this current flows via open drain SO1 or SO2. The maximum allowed SOx load current is 20mA.

![Diagram of optical interface driving a SCALE-2 gate driver core (example with 2SC0435T)](image)

Only direct mode is recommended (MOD is connected to GND) with the use of two or more SCALE-2 gate driver cores with direct paralleling (Fig. 6). The inputs INA and INB are connected in parallel. The SO fault outputs can be connected together, or each can be wired to a fiber-optics interface. A pull-up resistor must be placed as close as possible to the gate driver core. This resistor is calculated for a diode current of approximately 13mA and a maximum open collector current of 20mA per channel.

Note that both pins TB are paralleled. The resistor value of Rb given in the data sheet must therefore be divided by two to obtain the corresponding blocking time.
Disabling the Advanced Active Clamping

To disable the active clamping function, the ACLx input needs to be left open. Refer to the corresponding application manual.

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**Fig. 6** Optical interface driving paralleled SCALE-2 gate driver cores (example with 2SC0435T)

**Fig. 7** Disabling advanced active clamping by SCALE-2 (example with 2SC0435T)
**V\textsubscript{CE\text{sat}} detection with SCALE-2 gate driver cores (excluding 2SC0108T)**

**Desaturation protection with resistors**

The collector sense must be connected to the IGBT collector or MOSFET drain with the circuit shown in Figs. 8 and 9 in order to detect an IGBT or MOSFET overcurrent or short-circuit.

At an IGBT off-state, the driver’s internal MOSFET connects pin VCE\textsubscript{x} to pin COM\textsubscript{x}. The capacitor C\textsubscript{ax} is then precharged/discharged to the negative supply voltage, which is about -10V referred to VEx (red circle in Fig. 8 left). During this time, a current flows from the collector (blue circle in Fig. 8) via the resistor network and the diode BAS416 to VISO\textsubscript{x}. The current is limited by the resistor chain.

It is recommended to dimension the resistor value of R\textsubscript{vcex} in order to obtain a current of about $I\textsubscript{Rvcex}=0.6$-$1\text{mA}$ flowing through $R\textsubscript{vcex}$ (e.g. 1.2-$1.8\text{M}\Omega$ for VDC-LINK=1200V). A high-voltage resistor as well as series-connected resistors may be used. In any case, the minimum creepage distance relating to the application should be considered.

$$I\textsubscript{Rvcex} = \frac{(V\textsubscript{CE\textsubscript{x}} - V\textsubscript{ISO\textsubscript{x}})}{R\textsubscript{vcex}}$$  \hspace{1cm} \text{Eq. 1}

The reference voltage is set by the resistor R\textsubscript{thx}. It is calculated via the reference current (typically 150μA) and the reference resistance R\textsubscript{thx} (green circle in Fig. 8)

$$V\textsubscript{refx} = 150 \mu\text{A} \cdot R\textsubscript{thx}$$  \hspace{1cm} \text{Eq. 2}

CONCEPT recommends the use of R\textsubscript{thx}=68kΩ to detect short-circuits. Lower resistance values make the system more sensitive and do not provide any advantages in the case of desaturated IGBTs (short-circuit).

**Fig. 8 VCE desaturation protection with resistors**

At IGBT turn-on and in the on-state, the above-mentioned MOSFET turns off. While $V\text{CE}$ decreases (blue curve in Fig. 8), $C\text{ax}$ is charged from the COM\textsubscript{x} potential to the IGBT saturation voltage (red curve in Fig. 8). The time required to charge $C\text{ax}$ depends on the DC bus voltage, the value of the resistor $R\text{ax}$ and the value of the capacitor $C\text{ax}$. For 1200V and 1700V IGBTs it is recommended to set $R\text{ax}=120k\Omega$. For 600V IGBTs the recommended value is $R\text{ax}=62k\Omega$. The resulting response time is given in the corresponding application manual. It is valid in the short-circuit condition for a minimum DC-link voltage of about $25V\cdot R\text{vcex}/R\text{ax}$. Note that the response time will increase for lower DC link voltages. However, the energy dissipated in the IGBT in the short-circuit condition generally remains at the same level or is even lower.

The diode D1 in Fig. 9 must have a very low leakage current and a blocking voltage >40V (e.g. BAS416). Schottky diodes must be explicitly avoided.
Desaturation protection with sense diodes

SCALE-2 technology also provides desaturation protection with high-voltage diodes as shown in Fig. 10. However, the use of high-voltage diodes has some disadvantages compared to the use of resistors:

- Common-mode current relating to the rate of change $\frac{dv_{ce}}{dt}$ of the collector-emitter voltage: High-voltage diodes have large junction capacitances $C_j$. These capacitances in combination with the $\frac{dv_{ce}}{dt}$ generate a common-mode current $I_{com}$ flowing in and out of the measurement circuit.

$$I_{com} = C_j \cdot \frac{dv_{ce}}{dt}$$  \hspace{1cm} \text{Eq. 3}

- Price: High-voltage diodes are more expensive than standard 0805/150V or 1206/200V SMD resistors.

- Availability: Standard thick-film resistors are comparatively easier to source on the market.

- Limited robustness: The reaction time does not increase at lower $V_{CE}$ levels. Consequently, false triggering may occur at higher IGBT temperatures, higher collector currents, resonant switching or phase-shift PWM, particularly when the reference voltage $V_{thx}$ is set lower than about 10V. The upper limit of the reference voltage is restricted to about 10V, which may lead to limited IGBT utilization: the collector current may be limited to values smaller than twice the nominal current, or the short-circuit withstand capability may be reduced.

During the IGBT off-state, D4 (and $R_{ax}$) sets the VCEx pin to COMx potential, thereby precharging/discharging the capacitor $C_{ax}$ to the negative supply voltage, which is about -10V referred to VEx. At IGBT turn-on, the capacitor $C_{ax}$ is charged via $R_{ax}$. When the IGBT collector-emitter voltage drops below that limit, the voltage of $C_{ax}$ is limited via the high-voltage diodes D1 and D2. The voltage across $C_{ax}$ can be calculated by:

$$V_{vax} = V_{CE sat} + V_{F(D1)} + V_{F(D2)} + \frac{(15V - V_{CE sat} - V_{F(D1)} - V_{F(D2)})}{(R_{ax} + 330\Omega)}$$  \hspace{1cm} \text{Eq. 4}

The reference voltage $V_{refx}$ needs to be higher than $V_{vax}$. The reference voltage is set up by the resistor $R_{thx}$. The reference voltage is calculated via the reference current (typically 150μA) and the reference resistance $R_{thx}$:

$$V_{refx} = 150 \mu A \cdot R_{thx}$$  \hspace{1cm} \text{Eq. 5}
It is recommended to use standard network diodes such as 1N4007 for D1 and D2 (2 diodes for 1200V IGBTs, 3 diodes for 1700V IGBTs). D3 and D4 must be high-speed diodes (e.g. BAS316). Schottky diodes must be avoided.

The value of the resistance $R_{ax}$ can be calculated with the following equation in order to program the desired response time $T_{ax}$ at turn-on:

$$R_{ax} [\Omega] \approx \frac{1000 \cdot T_{ax} [\mu s]}{C_{ax} [pF] \cdot \ln\left(\frac{15V + V_{GLx}}{15V - V_{refx}}\right)}$$

Eq. 6

$V_{GLx}$ is the absolute value of the turn-off voltage at the driver output. It depends on the driver load and can be found in the driver data sheet /3/.

Recommended high-voltage diodes D1/D2 and values for $R_{ax}$ and $C_{ax}$ are:

- High-voltage diodes: 2x 1N4007 for 1200V IGBT
  3x 1N4007 for 1700V IGBT
- $R_{ax}$=24kΩ...62kΩ
- $C_{ax}$=100pF...560pF

Note that $C_{ax}$ must include the parasitic capacitance of the PCB and the diode D3.

Note also that the instantaneous $V_{ce}$ threshold voltage is determined by the voltage at pin REFx (150μA through $R_{thx}$) minus the voltage across the 330Ω resistor as well as the forward voltages across D1 and D2.

Note that the minimum off-state duration should not be shorter than about 1μs in order not to significantly reduce the response time for the next turn-on pulse.

Example: A resistor of $R_{ax}$=$46k\Omega$ must be used to define a response time of 6μs with $C_{ax}$=150pF, $R_{thx}$=33kΩ and $V_{GLx}$=9V.
**Disable \( V_{CE\text{sat}} \) detection by SCALE-2 (excluding 2SC0108T)**

To disable the \( V_{CE\text{sat}} \) measurement of gate driver cores, a resistor with a minimum value of 1\( k \Omega \) needs to be placed between \( VCE\text{x} \) and \( COM\text{x} \).

The reference resistor \( R_{th\text{x}} \) may be chosen between 33\( k \Omega \) and infinity, i.e. the REF\text{x} pin may be left open.

---

**Minimum pulse suppression for inputs INA and INB**

SCALE-2 gate drivers feature very fast signal propagation delays of typically <90ns. This includes a minimum pulse suppression time of 35ns. This avoids false gate switching caused by possible EMI. Figure 12 illustrates how to increase the minimum pulse suppression time if the SCALE-2 internal minimum suppression time is not long enough.

Figure 12 shows that it is not recommended to apply a RC network directly to INA or INB as the jitter of the propagation delay may increase considerably. The use of a Schmitt trigger is recommended to avoid this drawback.

Note that it is recommended to parallel the inputs INA/INB of the drivers after the Schmitt-trigger inverters if direct paralleling is used together with minimum pulse suppression. The use of a Schmitt-trigger inverter for each driver core is not recommended by direct paralleling as the delay divergence of the Schmitt-trigger inverters may be too high, leading to an excessive dynamic current imbalance during IGBT commutation.

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**Fig. 11** Disabling the \( V_{CE\text{sat}} \) detection by SCALE-2 driver cores (example with 2SC0435T)
Fig. 12 Minimum pulse suppression for INA and INB for SCALE-2 driver cores

The \( R_1/C_1 \) combination together with a 15V Schmitt-trigger inverter CD40106 create minimum pulse suppression. As an example, the Schmitt-trigger input hysteresis is 5V if the turn-on level is 10V and the turn-off level is 5V. If INx turns on with 15V logic, the capacitor \( C_1 \) is charged by \( R_1 \). When the voltage across \( C_1 \) reaches 10V, the Schmitt trigger switches. If INx becomes low (turn-off command) and the voltage across the capacitor \( C_1 \) gets lower than 5V, the Schmitt trigger switches. In our example, we use two Schmitt-trigger inverters, so the input signals don’t need to be inverted.

The minimum pulse suppression time \( T_{\text{min, on}} \) at turn-on can be calculated as follows:

\[
T_{\text{min, on}} = R_1 \cdot C_1 \cdot \ln\left(\frac{V_{\text{DD}}}{V_{\text{DD}} - V_{\text{TH, \text{high}}}}\right) \quad \text{Eq. 7}
\]

where \( V_{\text{TH, high}} \) is the upper Schmitt trigger threshold and \( V_{\text{DD}} \) is the logic level of INx.

The minimum pulse suppression time \( T_{\text{min, off}} \) at turn-off can be calculated as follows:

\[
T_{\text{min, off}} = R_1 \cdot C_1 \cdot \ln\left(\frac{V_{\text{DD}}}{V_{\text{TH, low}}}\right) \quad \text{Eq. 8}
\]

where \( V_{\text{TH, low}} \) is the lower Schmitt trigger threshold and \( V_{\text{DD}} \) is the logic level of INx.

Example:
- For \( T_{\text{min, on}} = 500\text{ns}, R_1 = 3.3\text{k}\Omega, V_{\text{TH, high}} = 10V, VDD = 15V \), we get \( C_1 = 138\text{pF} \)
- For \( T_{\text{min, off}} = 1\mu s, R_1 = 3.3\text{k}\Omega, V_{\text{TH, low}} = 5V, VDD = 15V \), we get \( C_1 = 276\text{pF} \)
**Increase of the noise immunity at inputs INA and INB**

Typically, all SCALE-2 gate driver cores turn on the corresponding channels when INA/INB reaches a threshold voltage of about 2.6V. The turn-off threshold voltage is about 1.3V. So the hysteresis is 1.3V. In some applications with very high noise interference voltages, increasing the input threshold voltage helps to avoid irregular switching events. For this purpose, a voltage divider $R_2$ and $R_3$ is placed as close as possible to the gate driver core according to Fig. 13. The minimum distance between the voltage dividers $R_2$ and $R_3$ and the gate driver is essential to avoid inductive coupling on the PCB layout.

![Fig. 13  Increased threshold voltages INA and INB by SCALE-2 gate driver cores](image)

Example: Let $R_2$=3.3kΩ, $R_3$=1kΩ and $INA$=+15V at turn-on. Without $R_2$ and $R_3$, the gate driver turns on as soon as $INA$ reaches 2.6V. The voltage divider increases the turn-on threshold voltage to about 11.2V. The turn-off threshold voltage is now about 5.6V. In this example, the INA and INB signal drivers have to provide 3.5mA during the IGBT on-state.

**Use of SOx fault outputs**

The fault outputs SOx are capable of driving up to 20mA. The longer the distance to the microcontroller, the more EMC-sensitive does the SOx line become, because the usual controller input has high impedance. When no fault condition is detected, the SOx output has high impedance. Voltage spikes can therefore easily be induced. The use of pull-up resistor $R_4$ according to Fig. 14 (top) on the end of the SOx line near the microcontroller is not recommended. Two solutions shown in Fig. 14 (center and bottom) can address this issue:

1) Line drivers are placed near the SOx outputs of the driver according to Fig. 14 (center). It is recommended to use pull-up resistors with $R_4$$>1$kΩ to VCC. If a fault occurs, the corresponding SOx output is pulled to GND. It is recommended to place the resistors as close as possible to the gate driver. The 100Ω resistors protect the line drivers against EMI. The pull-down resistors $R_5$ protect the microcontroller inputs against voltage spikes.

2) A protection network made with 10Ω resistors and Schottky diodes protects the SOx outputs of the driver according to Fig. 14 (bottom).
**VEx terminal characteristics**

VEx corresponds to the emitter potential. It is an internally generated potential of a SCALE-2 ASIC. During normal operation, the voltage between the pins VISoX and VEx is regulated to a nominal value of +15V. This is done by means of a SCALE-2 internal current source and voltage measurement in the secondary ASIC IGD. Its maximum sink/source capability is limited to ±2.5mA in order to avoid thermal overloading of the ASIC during operation.

If the secondary voltage between VISoX and COMx begins to fall, the voltage between VISoX and VEx remains constant at 15V in a first step. The voltage between VEx and COMx is reduced up to about 5.5V. If the voltage still falls from VISoX to COMx, the voltage from VEx to COMx remains constant at 5.5V and the
voltage from VISOx to VEx begins to fall. This function ensures a proper turn-off of IGBTs even in the event of a supply undervoltage.

No static load should be applied between VISOx and VEx or between VEx and COMx in order not to disturb the +15V regulation between VISOx and VEx. A static load can be applied between VISOx and COMx if necessary (e.g. supply load for external electronic functions). This is illustrated in Fig. 15.

![Fig. 15](image1.png)

*Fig. 15  Allowed external loading of VISOx, VEx and COMx (example with 2SC0435T)*

Note that it is not permitted to insert a resistor between the gate and emitter as shown in Fig. 16, as this would also statically load the +15V regulator.

![Fig. 16](image2.png)

*Fig. 16  Impermissible resistor between gate and emitter (example with 2SC0435T)*
The voltage at VEx (and therefore the gate-emitter voltage) can also be set to a custom specific value by means of external circuitry. The internally controlled 2.5mA DC current at VEx is then drawn/sourced by external components such as a combination of a resistor with a Zener diode or by a linear regulator. Note, however, that switching VEx to COMx during operation is not allowed and may lead to driver failure.

**Required blocking capacitors C1x and C2x**

The SCALE-2 gate drivers are equipped with blocking capacitors on the secondary side of the DC/DC converter (for values, refer to the corresponding driver data sheet /3/). These blocking capacitors allow fast charges and discharges of the gate capacitance of power semiconductors (which is characterized by the gate charge) via the N-channel MOSFET driver stages.

For IGBTs or MOSFETs, a minimum total blocking capacitance of 3µF is recommended for every 1µC of gate charge. The missing blocking capacitance on a SCALE-2 driver core must be added externally.

The blocking capacitors must be placed between VISoX and VEx (C1x in Fig. 17) as well as between VEx and COMX (C2x in Fig. 17). They must be connected as close as possible to the driver's terminal pins with minimum inductance. It is recommended to use the same capacitance value for both C1x and C2x (IGBT mode). Ceramic capacitors with a dielectric strength >20V are recommended. Note that during power-on, the capacitors are charged with a limited current thanks to the soft start function implemented in the SCALE-2 gate drivers.

If the required capacitances C1x or C2x exceed the maximum value given in the corresponding description and application manual, please contact CONCEPT’s support service.

Note that the use of electrolytic capacitors such as tantalum capacitors is not recommended.

![Fig. 17  Use of external blocking capacitors on the secondary side (example with 2SC0435T)](image-url)
Rail-to-rail output and gate-emitter voltage clamping

CONCEPT SCALE-2 gate drivers use an N-channel output stage like that shown in Fig. 18. After charging the power semiconductor gate input, the voltage drop over the N-channel MOSFET is nearly zero. SCALE-2 drivers therefore feature rail-to-rail gate outputs.

A rail-to-rail output has several advantages in driving power semiconductors. The first one is that the VISOx voltage can be regulated to +15V. By using a Schottky diode (DS Fig. 18), the gate-emitter voltage is clamped to the regulated +15V. This avoids an increase of the external gate-emitter voltage and consequently lowers the IGBT short-circuit current I_sc and energy, as the former is highly dependent on the gate-emitter voltage V_ge:

\[ I_{sc} = f(V_{ge}) \]

Eq. 9

The gate-emitter clamping described here is much more efficient than gate-emitter clamping with transient voltage suppressors. The latter does not allow the gate-emitter voltage to be limited in the short-circuit condition to 15V, as some clamping voltage reserve must be applied in view of the component tolerances and temperature dependence in order to avoid static conduction and therefore overload at V_ge=15V.

A second advantage is that parasitic power semiconductor turn-on can be prevented when the gate driver power is off. In that case, the gate-emitter voltage on the power semiconductor is zero. If the collector-emitter voltage V_ce increases at a given dV_ce/dt, a current I_g will flow in the gate loop via the Miller capacitance C_Miller:

\[ I_g = C_{Miller} \cdot \frac{dV_{ce}}{dt} \]

Eq. 10

With the use of DS in Fig. 18 the current I_g will charge the blocking capacitors C12 and C22. The voltage over C12 and C22 will generally remain low. A parasitic turn-on of the power semiconductors is therefore not possible. This function can be also used for STO (Safe Torque Operation).

![Fig. 18 Rail-to-Rail output and gate-emitter clamping (example with 2SC0435T)](image)

Note that the gate-emitter clamping described here is not possible on 2SC0108T drivers since VISOx is not available externally. Gate-emitter clamping with transient voltage suppressors should be used instead.
In IGBT mode, the positive turn-on gate voltage is regulated to +15V and the negative turn-off gate voltage is negative, typically about -10V for SCALE-2 gate driver cores.

With the MOSFET mode, it is possible to set the turn-off gate voltage to 0V.

It is recommended to proceed in the following way to activate the MOSFET mode on SCALE-2 driver cores:

1) Connect the secondary-side terminals COMx and VEx together. This must be performed with the driver power supply turned off, otherwise the secondary ASIC IGD may be damaged. The blocking capacitors C21 on Fig. 19 may be used if required. The blocking capacitors C22 of Fig. 18 are no longer required as they are short-circuited.

2) Select the required gate-emitter voltage at turn-on. The primary-side supply voltage VCC still needs to be +15V. The secondary-side supply voltage VISOx to COMx can be adjusted from 10V to 20V with VDC. It corresponds to the gate turn-on voltage. The transfer ratio from VDC to VISOx-COMx is typically 1.67. The under-voltage lock-out on the secondary side changes from 12.6V in IGBT mode to 8.75V in MOSFET mode (typical value). A VDC voltage lower than about 5.2V typically produces an under-voltage fault in MOSFET mode. As an example, VDC=6V typically leads to a positive gate turn-on voltage of 10V. Note, however, that this value is dependent on the driver output power and the temperature.

3) The reference voltage Vth for VCE monitoring (to be programmed with Rth) must be set at values higher than or equal to 4V referred to COMx.

Note that the MOSFET mode has been designed for ultra-fast MOSFET switching. The switching delays can thus be reduced to a minimum. A single positive turn-on voltage is then necessary.

MOSFETs have low gate-emitter threshold voltages. The use of MOSFET mode is consequently not always recommended and depends on the application. The IGBT mode can be used to drive MOSFETs and avoid their parasitic turn-on thanks to the negative gate-emitter voltage in the off-state.
Paralleling a dual-channel driver to a single output

Dual-channel driver cores can be configured to a single driver core with the double output power and gate current.

It is recommended to proceed in the following way and as shown in Fig. 20 to merge both driver channels to one logical channel (excluding 2SC0108T):

- Direct mode must be selected (MOD pin pulled to GND).
- Both input signals INA and INB must be connected together.
- Both secondary-side emitter potentials VE1 and VE2 must be connected together.
- It is recommended to disable the desaturation protection for one channel while it is enabled on the other channel.
- The reference value $V_{th2}$ is set up to 10V with $R_{th2}=68k\Omega$.
- Both channels need gate resistors to decouple the driver output stages. The driver channels are connected together on the IGBT gate side of the gate resistors. The turn-on and turn-off gate resistors need to be the same for both channels with a tolerance value of $\leq 5\%$ (1% recommended).
- The active clamping controls the turn-off driver stages in the driver core at turn-off. Each of the Advanced Active Clamping pins ACLx of both channels must therefore be connected to a $20\Omega$ resistor according to Fig. 20.
- Both fault signals SO1 and SO2 can be connected to a single fault signal SO.
- As soon as a fault is detected at SO, the PWM input signal must be pulled to GND in order to turn-off any driver channel that may not already be turned off. Omitting this point could lead to thermal damage to the driver, as one driver channel is turned off in the fault condition and the other remains turned on, leading to high power losses in the driver. The PWM input should not be activated before the SO fault signal is high again, i.e. no fault signal is available. This is important in order to avoid only one channel switching, as the blocking time of both driver channels is not exactly the same.

![Fig. 20 Paralleling a dual-channel driver to a single output (example with 2SC0435T)](image-url)
Paralleling the two gate driver channels on 2SC0108T is similar to the procedure for all other SCALE-2 gate driver cores. The main difference is that no Advanced Active Clamping is available. If (basic) active clamping is used, the transient voltage suppressor chain is connected directly to the gate (see Fig. 21).

**Fig. 21** Paralleling both driver channels of 2SC0108T

### Disabling one channel for chopper applications

In some cases, a single gate driver is required, such as for chopper operation, e.g. a break chopper in a DC-link bus. A single gate driver is not always available or commercially viable for such applications. A dual-channel gate driver core can therefore be used where one channel has to be disabled.

It is recommended to proceed in the following way to disable one driver channel:

- The corresponding signal input INx must be pulled to GND.
- The fault feedback SOx can be left open.
- Direct mode must be selected (MOD pin pulled to GND).
- The secondary side of the channel can be left open (not connected).

### Position of the Gate Driver in the Converter

The temperature as well as both magnetic and electric fields can influence the functionality of the signal electronics. Choosing the right position for the gate driver in the power electronics system helps to prevent system dysfunction and EMI effects.

CONCEPT SCALE-2 gate drivers are generally designed for ambient temperatures of up to +85°C. Excessive temperatures mainly limit the DC/DC power. In the worst case, the DC/DC transformer core goes into saturation and the gate driver core is destroyed. In converters where the gate driver is placed close to the heat sink or the power semiconductors, it is important to check that the maximum permissible temperature around the driver is not exceeded.

Furthermore, high currents generate high magnetic fields and high voltages generate high electric fields. Combined with high switching speeds, these fields represent a harsh environment for the signal electronics available on the gate drivers. This point is further detailed below.
2SC0108T and 2SC0435T on top of 17mm IGBT modules

17mm IGBT modules are becoming increasingly popular in power electronics applications. Manufacturers like Fuji, Infineon, IXYS, Mitsubishi, Semikron and Danfoss Silicon Power offer a range of 17mm packages on the market.

It is not recommended to use 2SC0108T or 2SC0435T drivers directly on top of IGBT modules, and especially not on top of 17mm IGBT modules. Magnetic field coupling during turn-on and turn-off events and especially during IGBT short circuit can lead to malfunction of the driver.

AC and DC bus bar

Laminated DC bus bars generally produce low external magnetic and electrical fields due to their laminated structure. A gate driver can therefore be located on top or underneath the DC bus as long the insulation or the clearances are sufficient.

However, the situation concerning the AC or phase leg bus bar is different. The output current generates a magnetic field around the bus bar and the rate of change of the electric field is generally high. If the gate driver is placed directly underneath or above the AC bus bar, shielding may be necessary. This can be an iron plate (shielding for low frequencies) or a thick aluminum or copper plate (shielding for high frequencies). The eddy current flowing in the shield will partially compensate for the magnetic field generated near the gate driver.

However, it is usually recommended to maintain a minimum distance (several cm are generally sufficient) between the AC bus bar and the gate driver core to reduce the effect of the magnetic field on the driver. Generally speaking, the closer the conducting current and the signal electronics are to each other, the higher is the risk of electromagnetic influences.
Clearances and Creepage Distances for PCBs

The following considerations regarding clearance and creepage distances assume Pollution Degree 2 (PD2) and Overvoltage Category II (OV II) at an altitude of up to 2000m for several standards:

<table>
<thead>
<tr>
<th>Description</th>
<th>Rated creepage voltage for 1700V blocking voltage</th>
<th>Creepage distances</th>
<th>Rated impulse voltage for clearances</th>
<th>Clearance distance</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENS0178</td>
<td>Electronic equipment for use in power installations</td>
<td>1250V</td>
<td>Basic insulation: 6.3mm&lt;br&gt;Reinforced insulation: 12.6mm</td>
<td>Rated voltage: 1700V</td>
</tr>
<tr>
<td>IEC60664-1</td>
<td>Insulation coordination for equipment within low-voltage systems</td>
<td>1000V</td>
<td>Basic insulation: 5mm&lt;br&gt;Reinforced insulation: 10mm</td>
<td>Basic insulation: 6kV&lt;br&gt;Reinforced insulation: 8kV</td>
</tr>
<tr>
<td>IEC60077-1</td>
<td>Electric equipment for rolling stock</td>
<td>1200V</td>
<td>Basic insulation: 8.6mm</td>
<td>Basic insulation: 6kV&lt;br&gt;Reinforced insulation: 10kV</td>
</tr>
<tr>
<td>IEC61800-5-1</td>
<td>Adjustable speed electrical power drive systems</td>
<td>1250V</td>
<td>Basic insulation: 6.3mm&lt;br&gt;Reinforced insulation: 12.6mm</td>
<td>Basic insulation: 6kV&lt;br&gt;Reinforced insulation: 8kV</td>
</tr>
</tbody>
</table>

Tab. 1  Summary of required creepage and clearance distances according to several standards

Gate driver cores in applications at >2000m altitude

CONCEPT gate driver cores are developed according to ENS0178 standards for creepage and clearance distances. They also satisfy the requirements for creepage and clearance distances stipulated in IEC60664-1.

As an example, for the IGBT voltage class of 1700V, the European and international standards require a clearance distance of 12.3mm and a creepage distance of 12.6mm for reinforced isolation. CONCEPT SCALE-2 gate driver cores satisfy these requirements (see corresponding data sheets).

Although there is sufficient margin, it should be noted that these requirements presume an atmospheric pressure higher or equal to that at a maximum altitude of 2000m above sea level. For altitudes higher than 2000m, IEC60664-1, Table A.2 describes correction factors for the clearances at different altitudes and air pressures. For example, with a maximum rated insulation voltage of 1700V, the maximum altitude for a 2SC0108T driver is 2000m. As a consequence, the maximum permissible rated insulation voltage needs to be reduced or the next larger CONCEPT IGBT gate driver is required if the application operates at higher altitudes and the corresponding standards must be satisfied. Thus 2SC0435T drivers can operate according to the IEC standards up to an altitude of 2900m.

Note that neglecting these requirements can lead to the destruction of the IGBT drivers and the IGBT modules.
A properly designed PCB layout of the adapter boards for SCALE-2 IGBT driver cores is essential to ensure correct gate driver operation. Successful operation will be difficult if basic PCB design rules are ignored.

One important rule for PCBs designed for power electronics applications is that layers relating to different high-voltage potentials must never overlap as shown in Fig. 23. If this is the case, large coupling capacitances between the different high-voltage potentials will result, leading to excessive common-mode current $I_{\text{com}}$ on the PCB during switching operation. Moreover, the long-term isolation reliability may become problematic.

![Fig. 23 PCB layout of SCALE-2 driver adapter boards](image)

Equations 11 and 12 describe how to calculate common-mode currents $I_{\text{com}}$ relating to overlapping plains in different PCB layers during IGBT commutation with a rate of change of the collector-emitter voltage of $dV_{ce}/dt$:

$$C_{\text{PCB}} = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{l} \quad \text{Eq. 11}$$

$A$ is the area where high-voltage potentials overlap, $l$ is the distance between both PCB layers, $\varepsilon_r=5$, and $\varepsilon_0=8.85\text{pF/m}$.  

$$I_{\text{com}} = C_{\text{PCB}} \cdot \frac{dV_{ce}}{dt} \quad \text{Eq. 12}$$

Not only planes (e.g. ground or emitter potentials) are affected by these rules. All other signal lines with large switching potential differences must also satisfy this rule. A high-side collector potential should therefore – as an example – never cross a low-side gate signal on the PCB layout.

CONCEPT has developed the following basic boards to show how correct layouts for the driver cores can be realized:

2BB0108T for 2SC0108T (see www.igbt-driver.com/go/2BB0108T)
2BB0435T for 2SC0435T (see www.igbt-driver.com/go/2BB0435T)

Schematics, BOM and even the Gerber files of the layouts are available on the specified Internet pages. Figures 24 and 25 show these layout examples.
Fig. 24  PCB layout of CONCEPT basic board 2BB0108T

Fig. 25  PCB layout of CONCEPT basic board 2BB0435T
## Typical Application Failures

<table>
<thead>
<tr>
<th>Impact on the driver</th>
<th>Effect</th>
<th>Cause</th>
<th>Corrective Action</th>
</tr>
</thead>
</table>
| Primary-side DC/DC MOSFET destroyed or LDI ASIC destroyed (2SC0108T) | DC/DC overload | Excessive switching frequency  
High noise on INA or INB  
Partial discharge  
Short circuit in gate, emitter, VEx, VISOx or COMx  
Use of oversized gate/emitter capacitor C_{GE}  
Excessive gate charge Q_{g}  
LC gate oscillation  
Excessively high ambient temperature  
Defective ceramic capacitor | Select next powerful gate driver or reduce switching frequency  
EMI protection e.g. minimum pulse suppression  
Mostly PCB layout failure; check all clearance and creepage distances  
Assembly or layout failure |  
Calculate the power losses for C_{GE}  
Calculate the power losses for Q_{g}  
Remove excessive inductance in the gate loop  
Reduce the ambient temperature below 85°C  
Avoid mechanical damage by handling process or bending of PCB |
| LDI ASIC destroyed | VDD>16V  
Pull-up resistor value at SOx too small  
ESD handling  
Max. isolation voltage of 1700V exceeded | Limit VDD to 16V  
Increase the resistor value  
Improve ESD handling  
Reduce V_{ce} overvoltage e.g. with active clamping or change to a higher IGBT blocking voltage |  
Calculate the power losses for VDD  
Calculate the power losses for Q_{g}  
Remove excessive inductance in the gate loop  
Reduce the ambient temperature below 85°C  
Avoid mechanical damage by handling process or bending of PCB |
| IGD ASIC destroyed | Excessive Advanced Active Clamping feedback (>3us) | Excessive DC-link voltage  
Excessive stray inductances | Overall design failure, change to higher IGBT blocking voltage  
Improve the DC bus bar (reduced stray inductance); do not apply current >40mA (mean value) to the ACLx pin |
| IGD ASIC destroyed | VISOx > 30V | Limit VDC to 16V |  
Calculate the power losses for VISOx  
Calculate the power losses for Q_{g}  
Remove excessive inductance in the gate loop  
Reduce the ambient temperature below 85°C  
Avoid mechanical damage by handling process or bending of PCB |
| Short circuit with destruction of LDI, IGD or DC/DC MOSFET | Crack of ceramic capacitors | Handling process, mechanical destruction; can also happen in final mechanical assembly process | Careful mechanical handling and assembly process |
| Delay divergence of gate signals between parallel connected IGBTs (>25ns) or jitter >5ns | Increased initial propagation delay | Use of half-bridge mode  
Slow rise and fall times applied to driver inputs | Use of direct mode  
Insert Schmitt-trigger gates to INA/INB |
Application Note

Bibliography

/2/ “Description and Application Manual for SCALE Drivers”, CONCEPT
/3/ Data sheets of SCALE-2 driver cores, CONCEPT
/4/ Application note AN-0901: Methodology for Controlling Multi-Level Converter Topologies with SCALE-2 IGBT Drivers, CONCEPT
/5/ Application note AN-0904: Direct Paralleling of SCALE-2 Gate Driver Cores, CONCEPT

Note: These papers are available on the Internet at www.IGBT-Driver.com/go/papers

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Manufacturer

CT-Concept Technologie AG
Intelligent Power Electronics
Renferstrasse 15
CH-2504 Biel-Bienne
Switzerland

Tel. +41 - 32 - 344 47 47
Fax +41 - 32 - 344 47 40

E-mail Info@IGBT-Driver.com
Internet www.IGBT-Driver.com