cadence®

Developing High-Frequency integrated circuits for test and measurement

By Cadence Design Systems

As a vendor for high-end test and measurement solutions used in mobile radios and radio communication, Rohde & Schwarz depends on the availability of proprietary ASICs delivering key functionality and performance. The IC design engineers at Rohde & Schwarz make extensive use of an Accelerated Parallel Simulator (Virtuoso®-APS) package to efficiently perform the complex simulations required to meet the demanding specifications of their high-frequency circuits. The development of high-frequency circuits is very demanding, in multiple dimensions; not least, in order to meet tight time-to-market schedules, the use of efficient development systems is a must. Rohde & Schwarz' application of this circuit simulator provides the company's engineers with a number of unique features that allow them to obtain results in a very efficient way.

PERIODIC NOISE ANALYSIS

A simulation method that designers frequently use for low noise frequency dividers and phase detectors is Periodic Noise (PNoise) Analysis. PNoise Analysis is very similar to the traditional Noise Analysis that is offered by all circuit simulators derived from the original Berkeley SPICE. However, whereas Noise Analysis simulates the circuit at a static DC operating point, PNoise Analysis simulates the circuit for a periodic state that is the result of a Periodic Steady-State (PSS) Analysis. As a consequence, frequency-translating effects such as mixing and sampling are automatically included in the results of a PNoise Analysis.

PNoise Analysis can be used for all circuits with periodic behaviour. Like the traditional Noise Analysis, it offers a Noise Summary, which is a list of noise sources sorted by the magnitude of their noise contribution to the circuit output. This list makes it very easy to identify possibilities for further reducing the noise of the circuit. PNoise Analysis also offers specialised analysis modes for the jitter of the rising or falling edge of a signal and for amplitude and phase noise. These analysis modes are essential for the precise simulation of circuits such as low noise frequency dividers and phase detectors and are used very intensively by Rohde & Schwarz.

TRANSIENT NOISE ANALYSIS

An alternative method for the noise simulation of a circuit that does not have a static DC operating point is the Transient Noise Analysis. This analysis does not require the circuit to exhibit periodic behaviour. It works by adding pseudo-random voltage and current sources with the appropriate effective value to all noise-generating components. The drawback of this approach is that it is not possible to obtain the very useful Noise Summary mentioned above. Typically, the circuit requires long simulation run times to obtain statistically meaningful results. For these reasons, the IC design engineers of Rohde & Schwarz prefer to use PNoise Analysis and almost never use Transient Noise Analysis.

The low-noise frequency dividers and phase detectors developed by Rohde & Schwarz are designed to operate over a large frequency range. This leads to special challenges when the noise performance must be simulated for low-frequency signals. This arises because, in PNoise Analysis, noise contributions are only taken into account from a specified number of sidebands. Noise coming from higher frequencies than the specified multiple of the fundamental frequency will be neglected. This means that for low-frequency

signals in wideband circuits, a very large number of sidebands must be specified in order to cover the entire bandwidth and to obtain accurate results. As the time required for PNoise Analysis is approximately proportional to the specified number of sidebands, this can lead to extremely long simulation times. Cadence has recently addressed this challenge by introducing the new full-spectrum option for the PNoise Analysis in Virtuoso-APS. With this new option, noise from white noise sources is taken into account over the entire frequency spectrum. Noise from coloured noise sources such as flicker noise is still only taken into account from a specified number of sidebands, but in this case a very low number of sidebands is usually sufficient for good accuracy. For Rohde & Schwarz, the new full-spectrum option has reduced the time required for PNoise Analysis with low frequency signals by a factor of up to 20. Analyses, at even lower frequencies, that were not possible to run before due to excessive simulation times can now be performed in a reasonable time contributing to a good chance of first-time-right silicon.

SMALL-SIGNAL ANALYSIS MODE

PNoise Analysis is not the only analysis type that simulates the circuit for a periodic state given by the result of a PSS Analysis. The PAC and PXF Analyses are small signal analyses equivalent to the AC and XF Analyses known from Berkeley SPICE or its derivatives. Like PNoise Analysis, they include frequency-translating effects such as mixing and sampling, which makes them ideal for simulating circuits like mixers or switched-capacitor filters. They also offer specialised analysis modes such as Sampled Analysis for jitter or Modulated Analysis for amplitude and phase modulation. Two more analysis types based on the results of a PSS Analysis are the Periodic Stability (PSTB) Analysis for simulating the loop gain of a periodic circuit and the Periodic Scattering Parameter (PSP) Analysis for simulating the S-parameters of frequency-translating circuits such as mixers.

Besides the Sampled and Modulated Analyses, PAC Analysis offers some additional specialised analysis modes. Of these, the Rapid IP3 Analysis has recently been very useful for the IC design engineers at Rohde & Schwarz. Rapid IP3 Analysis is a method that calculates the third-order intermodulation (IP3) of a weakly-nonlinear mixer circuit with the computational effort of five PAC simulations. Alternative methods for calculating the IP3 of a mixer require a much higher computational effort because the circuit must be simulated with at least two signals applied simultaneously at different frequencies.

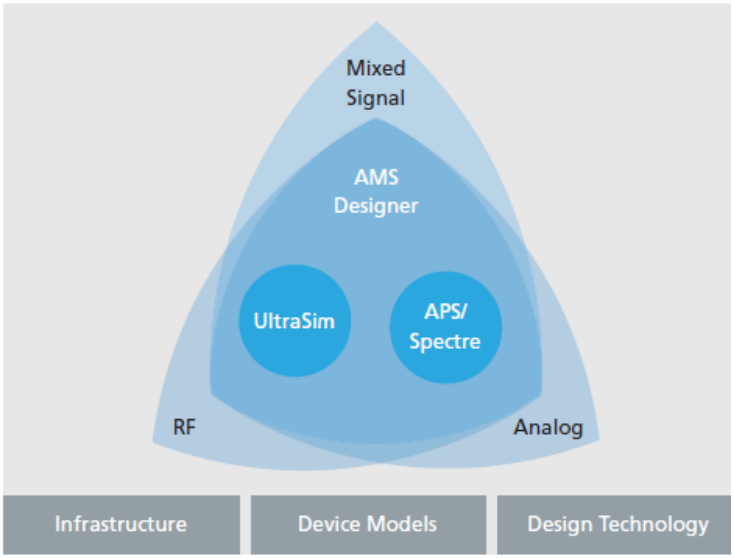
In the case described here, Rohde & Schwarz had to simulate the IP3 of a mixer that contained an extremely large number of parasitic components that had been extracted from the (physical) layout. A PSS Analysis with a signal at a single frequency was still possible, but attempts to introduce a second frequency caused the simulation to exceed the available computer memory. However, by using Rapid IP3 Analysis, Rohde & Schwarz was able to determine the third-order intermodulation of the mixer, something that would have been impossible otherwise.

Another advanced feature of Virtuoso-APS that Rohde & Schwarz designers use extensively to ensure the reliability of all of their circuits is the analogue asserts. All components used in integrated circuits have maximum voltage and current ratings that may not be exceeded, in order to avoid destruction or a reduction of lifetime. However, violations of these maximum ratings are very easily missed in normal simulations. Analogue asserts allow designers to specify these limits in a general way and then to perform an automatic compliance check for all components during all simulations. All violations are reported, together with the name of the component and the time at which the event occurred so that they can be examined in further detail.

A feature of analogue asserts in the Cadence tool set is that arbitrary expressions containing the values of component parameters can be used for calculating the permitted voltage and current ratings. For example, the maximum current rating of a resistor will usually depend on its (physical) width due to the maximum allowable current density of the material in which is formed. Virtuoso-APS allows a very simple specification of such variable limits, so analogue asserts have become a standard tool for the IC design engineers at Rohde & Schwarz.

EXPLOITING MULTI-CORE HOSTS

As its name already implies, the Accelerated Parallel Simulator contains a parallel matrix solver that allows a very efficient use of modern multi-core processor architectures and a corresponding speedup of time-consuming simulations. A token-based licensing system permits a very flexible use of these capabilities depending on simulation size, CPU load of the computer, and available license resources. Rohde & Schwarz uses the flexible licensing system to control costs while using additional products such as Virtuoso AMS Designer (a mixed-signal simulator) and Virtuoso UltraSim (a FastSPICE simulator).



Virtuoso Multi-Mode Simulation offers a complete verification solution for silicon realization

In order to realise high-performance test and measurement equipment specifications in its instrumentation product range, Rohde& Schwarz has to develop its own proprietary integrated circuits if components with the required performance are not available on the market; in the T&M sphere, this is frequently the case. Gerhard Kahmen, director of the Mixed-Signal IC Design Subdivision of Rohde & Schwarz, says: “The Virtuoso Accelerated Parallel Simulator from Cadence Design Systems offers a number of unique features that enable us to thoroughly evaluate our high-performance integrated-circuit designs and at the same time meet tight time-to-market schedules. The new features recently introduced to Virtuoso-APS have allowed us to improve our productivity even further and to increase our chance of first-time success.”

The Accelerated Parallel Simulator (Virtuoso-APS) is a part of the Virtuoso Multi-Mode Simulation (Virtuoso- MMSIM) tool suite and is used for the simulation of analogue and high-frequency circuits for next-generation products.

Virtuoso Accelerated Parallel Simulator

Virtuoso Accelerated Parallel Simulator, a key component of the Virtuoso Multi-Mode Simulation, provides advanced performance for the next generation of analog and RF simulation. It delivers significant scalable performance and capacity at full Spectre accuracy across a broad range of complex analog, RF and mixed-signal blocks, and sub-systems with sizes up to millions of transistors and passive and parasitic elements. Virtuoso Accelerated Parallel Simulator provides all the transistor-level analysis capabilities available in Virtuoso Spectre Circuit Simulator. Additionally, its proprietary parallel simulation technology delivers scalable multi-core processing capability on modern multi-core compute platforms.

Benefits

Provides significant single-core performance with an identical use model and full Spectre accuracy for everyday simulation of complex and/or large block designs, leading to faster convergence

Enables high-precision simulation for large post-layout analog and RF designs and subsystems dominated by parasitic devices

Delivers scalable performance leveraging a single machine or cluster of machines with multi-core architectures, allowing higher levels of analog design integration and verification and a quick turnaround time on simulation

Enables fast and accurate analysis of complete transceivers and large post-layout RF IC blocks by significantly improving the performance and capacity of harmonic balance analysis using a multi-core compute platform

Features

Supports all analyses offered in the Virtuoso Spectre Circuit Simulator

Offers advanced parallel simulation on a single multi-core compute platform

Supports distributed, advanced parallel simulation across a cluster of multi-core compute platforms

Provides parasitic stitching and reduction for post-layout design and verification, providing additional performance gain for analog and RF designs dominated by parasitics

Multi-core harmonic balance and envelope analysis

Full support of RF components and measurements library with identical-use model to standard RF simulation capabilities in the Virtuoso Spectre environment