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Understanding the Effect of Power MOSFET Package Parasitics on VRM Circuit Efficiency at Frequencies above 1MHz

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Abstract

The effect of frequency on the parasitic inductance and resistance of DPAK, D2PAK, MLP, SO-8 and the proprietary DirectFET™ power package are presented. Each package shows a characteristic increase in resistance with frequency in the range of 100KHz to 5MHz. The observed trend in resistance with frequency is expected to be a consequence of the skin effect phenomenon. The DirectFET™ package exhibits the lowest inductance and resistance at frequencies up to 5MHz. The effect of package parasitics upon in circuit VRM efficiencies is presented by comparing circuits containing near identical active area silicon housed in SO-8 and DirectFET™ packages. VRM circuits containing the DirectFET™ devices display higher efficiency than those assembled with SO-8's. The difference in VRM efficiency between the two circuits increases with frequency over the range of 800KHz to 2 MHz. This trend is expected to be a consequence of the lower parasitic impedance of the DirectFET™ package. In circuit switching waveforms captured from both circuit are discussed and used to validate package inductance measurements.

Introduction

Over the past decade the transistor count within microprocessors has continued to increase in line with Moore's law [1]. Over the same time period improvements in device geometry and reduced transistor gate lengths have enabled operating frequencies to increase from a few tens of MHz to over 2GHz. Microprocessor power requirements have also increased significantly from a few amps to over 50 amps. The fast transient current response times demanded by microprocessors has lead to the adoption of point of load converters and voltage regulator modules (VRM). These modules convert power from a fixed supply rail, to the 1.x Volts required by the microprocessor.

Figure 1. Range of packages investigated. From left to right: D2PAK, DPAK, SO-8, MLP and DirectFET™

There are several benefits to increasing the operating frequencies of VRM designs. The passive component values on the input and output stages of the VRM can be reduced and in many cases space savings can be realized. The parasitic impedances of conventional power electronic packages operating at frequencies over 1MHz are not well characterized. In this paper the parasitic inductance and resistance of a range of power electronic packages are presented and compared to the proprietary DirectFET™ package [2,3] over the frequency range of 500KHz to 5MHz. The packages examined are the DPAK, D2PAK, SO-8, MLP and DirectFET™. The packages, shown in figure 1, were assembled in die free form, in order to aid comparison on a like for like basis. To demonstrate the effect of package parasitics upon VRM in-circuit efficiencies, near identical silicon housed into SO-8 and DirectFET™ packages have been assembled into 2 phase VRM circuits. The efficiency of these circuits is compared over the range of frequencies 500KHz to 2MHz. Switching waveforms captured across each of the packaged devices are presented in order to demonstrate the effect of package inductance upon switch node ringing. Finally this data is used to validate the ratio of die free package inductance measurements presented in this paper.

Die free package and test card assembly

DPAK, D2PAK, SO-8 and MLP packages were assembled die free. In each case the wirebonds conventionally used in each package were positioned on the same X-Y coordinates of the die bonding paddle as they would normally occupy with silicon in place. In the case of the DirectFET™ package, the silicon die was replaced by a stamped copper die of equivalent dimensions to the largest silicon die that can be assembled within the package. It was necessary to place the copper die within this package in order to make contact from the land patterns on the test cards (described below) to the under side of the DirectFET™ 'can' assembly. The copper die was attached to the underside of the 'can' using identical conductive die attach adhesive to that used in the standard DirectFET™ assembly process.

Test cards were fabricated from double sided FR4 with 2 Ounce copper tracking. Packages were assembled onto the test cards using no clean Sn62Pb36Ag2 near eutectic solder (Multicore SN62MP100AGS90). The solder was screen printed onto test cards prior to pick and place and re-flowed using a JEDEC standard profile. Each assembly was then inspected for defects.

Parasitic impedance test methodology

Package parasitic impedances were measured using an Agilent 4285A precision LCR meter. A custom test interface was developed in order to allow the LCR meter to accept the device test cards described below. Resistance, R, and reactance, X, values were measured at each frequency using the following protocol:

1) Insert 'open circuit test card' into test fixture & perform OPEN circuit correction
2) Insert 'short circuit test card' into test fixture & measure SHORT circuit R and X values
3) Insert device under test card into test fixture and measure LOAD R and X

At each frequency inductance values were extracted from reactance using the relationship, X = j?L, where, L, is the inductance and, ?? is the angular frequency. It should be noted that the precision LCR meter was operated in the correction mode for improved low resistance repeatability.

Parasitic measurement test card design

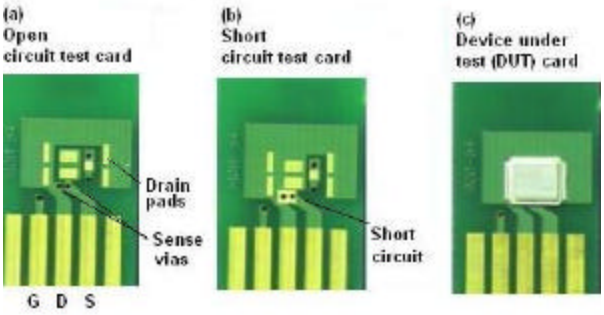


Figure 2. Example of test cards used to characterise DirectFET™ package

The test cards used to extract parasitic impedances from the DirectFET™ packages are shown in figures 2(a), (b) and (c). Figure 2(a) shows the OPEN circuit test card used to back correct the LCR meter sense pins. Current was forced through the front side gate, drain, and source connections labelled G, D and S respectively. Sense vias were routed along the rear side of the test cards (not shown). Figure 2(b) shows the short circuit test card and Figure 2(c) shows the device under test, or DUT, test card. In order to obtain low resistance short circuit measurements the drain and source sense via holes were located as close together as possible as shown in figure 2(b). The resultant short circuit obtained between sense vias was calculated to be approximately 40 ?Ohms. It should be noted that the track impedances from the sense vias to the land pads of the devices under test are included in all of the experimental results shown below. The results presented below are therefore for board mounted packages, <u>not</u> discrete packages. The test card designs for each of the packages investigated are shown in figure 3. The red circle superimposed onto each of the images highlights the location of the sense vias. Every effort was made to ensure the sense vias were placed as close to the device under test as possible in order to reference out as much track impedance as possible in the measurements.

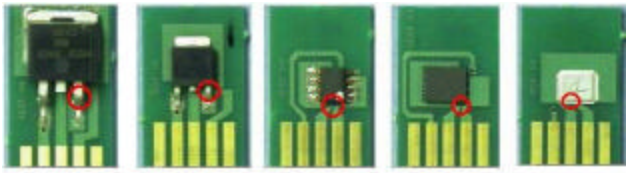


Figure 3. Example of test cards used to characterise (from left to right) D^{2}PAK, D-PAK, SO-8, MLP and DirectFET™ packages.

Comparison of package impedance characteristics

Figure 4 shows the die free package resistance versus frequency for the range of die free packages tested. At frequencies of a few hundred KHz the DirectFET™ and D2PAK packages have the lowest board mounted resistance at approximately 600?Ohm and 1.5 mOhm respectively. DPAK, MLP and SO-8 exhibit much higher board mounted resistance at over 2 mOhms. As the frequency increases all packages show an increase in board mounted die free package resistance with frequency. At 2 MHz for example, the DirectFET™ board mounted package resistance is approximately 1.2mOhms. All the other board mounted packages characterized here have over 3 mOhms resistance at this frequency.

Figure 5 shows the board mounted die free package inductance versus frequency for the range of packages characterised. At frequencies in the region of 200KHz the D2PAK exhibits the highest inductance. This is followed, in order of decreasing inductance, by the DPAK, SO-8/MLP and DirectFET™ packages. The DirectFET™ package exhibits the lowest inductance of all devices tested. All packages characterised show a decrease in inductance with frequency over the range of 200KHz to 5 MHz.

The mechanism behind the increase in board mounted die free package resistance with frequency is expected to be a consequence of the skin effect phenomenon [4]. Skin effect is an electromagnetic phenomenon in which current flowing through a material of a given cross sectional area is confined to the perimeter of that area at elevated frequencies. For a flat plate of copper, or wire bond, the skin depth is given by the equation [4]:

$$? = (?/? ?_o f)^{1/2} \qquad \ldots(1)$$

Where ??is the skin depth in m??? ?is the material resistivity, $?_o$ is the permeability of free space and, f, is frequency. As a rule of thumb, all current is normally constrained within approximately three skin depths. Figure 6 shows the variation in skin depth with frequency for three common metals utilised in power electronics packaging; copper, aluminium and gold. At a frequency of 1MHz the skin depth for copper is approximately in the region of 60 um. This is significantly lower than the typical leadframe thickness of an SO-8 device for example, which is in the region of 250um.

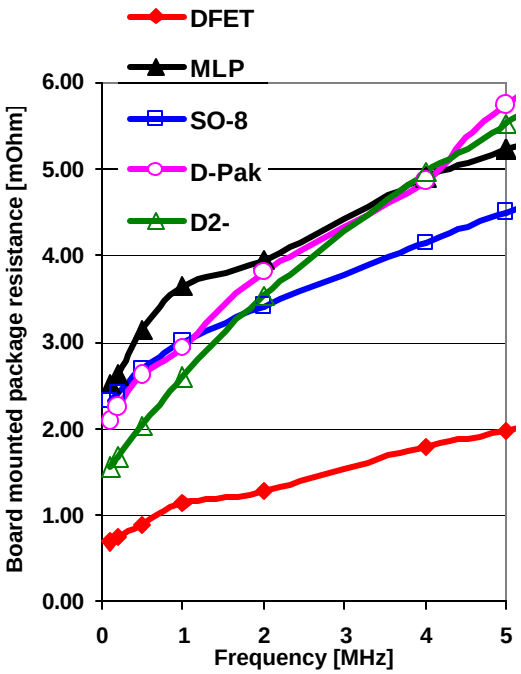


Figure 4. Die free package resistance versus frequency

The frequency dependence of the resistance and inductance of a rectangular shape of metal or circular cross section wire can be modelled using Maxwell's equations. Resistance can be shown to be a function of the ratio of plate thickness, t, over skin depth, ? [5]. Figure 7 shows the modelled ratio of ac to dc resistance, Rac/Rdc, of various plate and wire geometries versus frequency. The geometries shown are common in power electronic

packaging. For example, 250um copper plate geometries are common in SO-8 leadframe assemblies, 250um aluminium wire is commonly used in DPAK and D2PAK packages and 25um diameter gold wire is typically utilised in SO-8 and MLP packages.

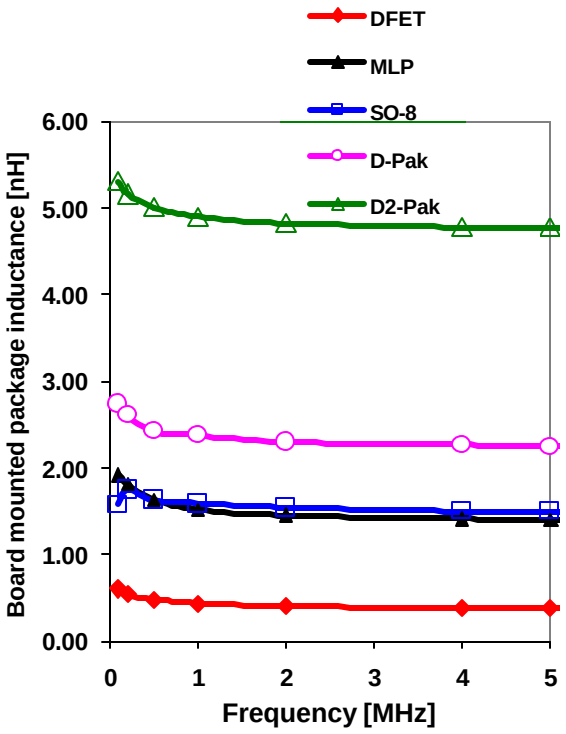


Figure 5. Die free package inductance versus frequency

It is clear from the modelled data in figure 7 that the resistance of materials that have greater diameter or thickness is more likely to increase with increasing frequency. For example the resistance of 25 um diameter gold wire remains relatively constant with frequency whereas the resistance of the 250 um diameter Aluminium wire and 250 um copper plate geometries increases by a factor of 2.5 or more as the frequency approaches 5MHz. This modelled data whilst only based upon approximations highlights that resistance does show an increasing trend with frequency as observed in the experimental data shown in figure 4.

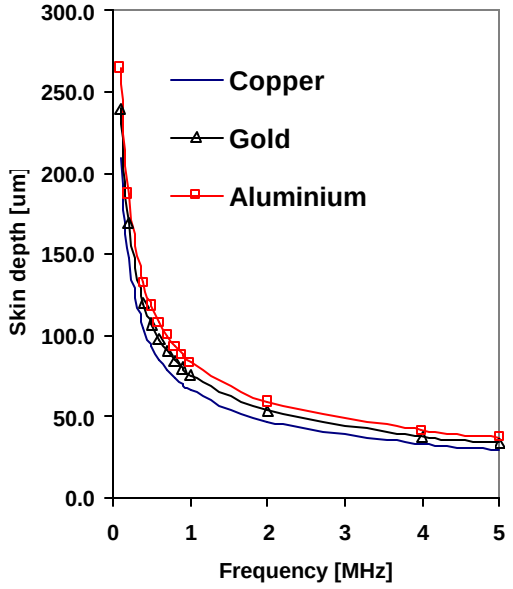


Figure 6. Skin depth versus frequency

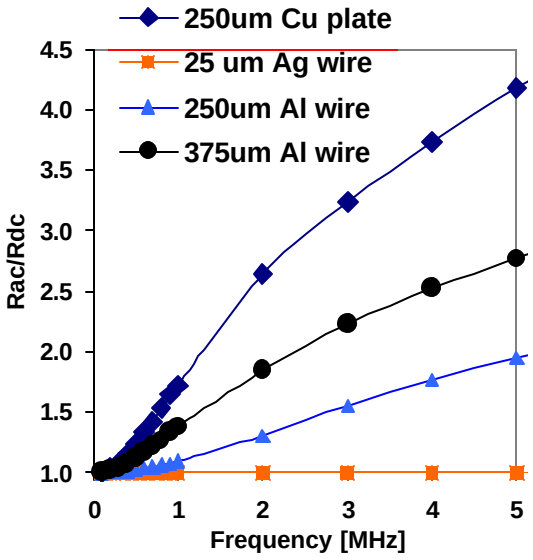


Figure 7. Modelled resistance versus frequency for commonly used power electronic packaging materials

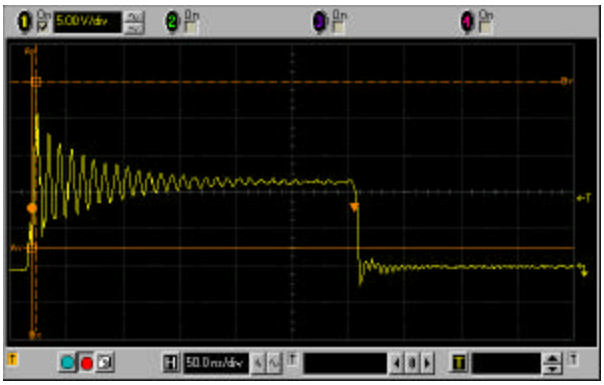
The effect of package parasitics on VRM in circuit performance

To highlight the effect of package parasitics on switching performance, silicon of the near identical active area, identical blocking voltage and generation was assembled into SO-8 and DirectFET™ packages. These devices were mounted onto 2-phase 1U VRM circuits. The circuits were operated at 500KHz per phase, output current 30A total (15 amps per phase). Drain to source voltage switching waveforms of the SO-8 and DirectFET™ devices operating in the synchronous FET position were captured and are shown in figures 8(a) and (b) respectively. With reference to figures 8(a) and (b), the SO-8 device has significantly more voltage ringing than the DirectFET™ device during turn off.

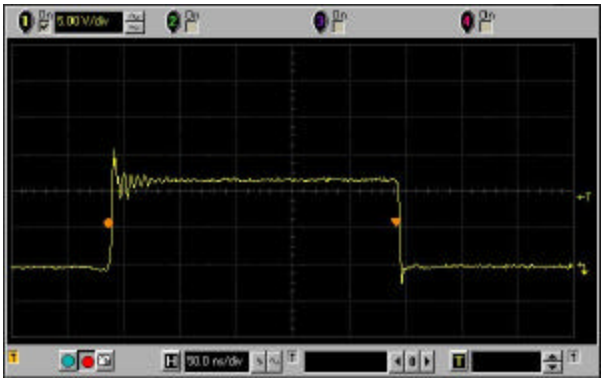
The ratio of the SO-8 package inductance to that of the DirectFET™ was estimated by inserting the peak voltage swings into the equation, V = LdI/dt. Using this approximation a ratio of 0.32 was obtained which is very close to ratio of experimentally determined board mounted inductances, 0.31, extracted from figure 5 above.

Reducing the effects of package parasitics can be used to increase VRM operating frequencies. Figure 9 shows the efficiency versus frequency curves of DirectFET™ and SO-8 devices operating in 2-phase VRM circuits. In both sets of devices the silicon technology, blocking voltage and active areas were kept near identical. Both circuits were cooled using a heatsink attached directly to the underside of the circuit boards. A positive airflow of 400LFM was directed onto the heatsinks during the efficiency measurements.

The VRM circuits containing DirectFET™ packaged silicon show higher efficiencies across the frequency range in comparison to their SO-8 counterparts. It is also noted that the difference in efficiency between the two circuits increases with increasing frequency favouring the DirectFET™ packaged silicon. This result reflects the reduced package parasitic losses in the DirectFET™ devices relative to those of the SO-8. DirectFET™ packaged devices were also able to operate under higher load current conditions. For example at 1MHz the DirectFET™ VRM circuits were able to switch up to 60A whilst maintaining a board temperature of less than 100C. SO-8 devices were only capable of switching in the region of 40A under identical operating conditions. The higher current handling capability of the DirectFET™ populated VRM circuits is attributable to the lower package parasitics and the increased thermal performance of the package.



8(a) SO-8 waveform



(b) DirectFET™ waveform

Figure 8. Synchronous FET switching waveforms of (a) SO-8 and (b) DirectFET™ devices in 1U VRM circuits utilising near identical active area silicon.

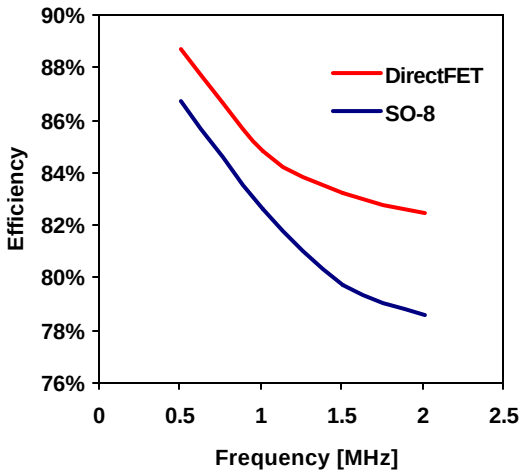


Figure 9. VRM in circuit efficiency versus frequency for DirectFET™ and SO-8 devices containing near identical silicon active area. Output current = 30A

The construction of the DirectFET™ package allows heat to be removed directly from the top of the package 'can' assembly as well as through the drain land pads into the circuit board [4,5]. Effective removal of heat though the top side of SO-8 packages is limited due to the presence of mould compound between the ambient and silicon active area. In the SO-8 devices the majority of heat is therefore removed through the package leads into the circuit board.

Conclusions

The parasitic impedances of DPAK, D2PAK, SO-8, MLP and DirectFET™ power electronic packages have been characterised over the frequency range of 500KHz to 5MHz. The DirectFET™ package has been shown to have the lowest board mounted die free package resistance and inductance over this frequency range. All packages show an increase in board mounted package resistance with frequency. This is expected to be a consequence of the skin effect.

The effect of package parasitics upon VRM circuit efficiency has been studied by comparing VRM circuits assembled with near identical silicon housed in DirectFET™ and SO-8 packages. The circuits containing DirectFET™ packaged silicon show over 1% improvement in efficiency at 500KHz over the SO-8 based solution. As the frequency increases to 2MHz this difference in efficiency extends to over 3.5%. This is expected to be a consequence of the lower package inductance and resistance of the DirectFET™ package compared to the SO-8. Switching waveforms of DirectFET™ housed silicon show significantly less ringing in circuit than silicon housed in SO-8 packages. This is a consequence of the lower inductance of the DirectFET™ package.

References

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