SyncE and IEEE 1588: Sync Distribution For A Unified Network

1. Introduction

Ethernet has become the preferred method of data transport over the last few decades because of its low operation cost and universal adoption in both enterprise and residential markets. It was a natural step for its application in the wide area network (WAN) which has been historically dominated by synchronous networks (e.g. SONET/SDH). Since Ethernet or packet based networks operate asynchronously, it cannot support many of the traditional applications that depend on synchronization such as circuit switched services and wireless backhaul. Synchronous Ethernet (SyncE) and packet timing using the IEEE 1588 protocol are key solutions to the transport of frequency synchronization over packet networks which will ultimately drive the interoperability of carrier Ethernet and legacy networks. This application note examines why frequency synchronization is necessary when transferring data within a SONET/SDH network and how packet networks transfer data without any synchronization. We will look at methods for transporting synchronization and propose potential synchronized timing implementations.

Most of the discussions in this application note will be based on a hypothetical network which is shown in Figure 1. The core of the network is based on asynchronous packet nodes, with synchronous SONET/SDH network elements transporting services closer to the edge of the network, eventually reaching end applications through customer premise equipment (CPE). The challenge with this network topology is enabling the asynchronous packet network to communicate with the synchronous SONET/SDH network elements. Before exploring possible solutions it is important to understand why synchronization is necessary when transferring data within SONET/SDH equipment, and why it is not in packet networks.

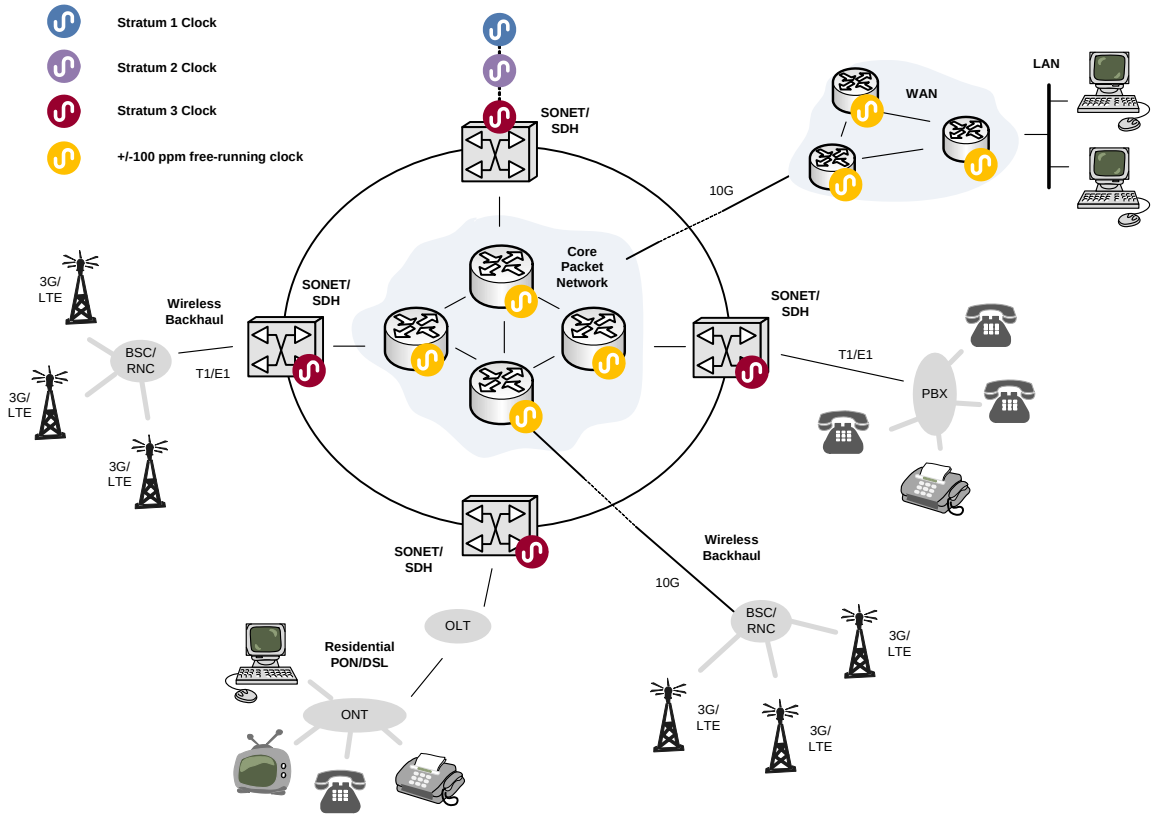


Figure 1. Example Network with Mixed Synchronous and Asynchronous Equipment

1.1. Synchronization of SONET/SDH Networks

Networks based on time division multiplexing (TDM), such as SONET/SDH or PDH, require precise frequency synchronization at each of its data interfaces for efficient transfer of information. In fact, without frequency synchronization, many of the services being carried over TDM networks would suffer or simply fail to work. An example of two SONET/SDH Network Elements (NE) communicating with each other is shown in Figure 2. Both the transmitting network element (TX NE) and the receiving network element (RX NE) operate from their own local clock frequencies (i.e., TX Local Clock and RX Local Clock) which are both synchronized to the same frequency source (an atomic clock or stratum 1 reference).

Data is exchanged from the TX NE to the RX NE through a slip buffer which is essentially a dual port memory. Data is written to the slip buffer using the TX NE's recovered clock frequency, and read out of the slip buffer at the RX NE's local clock frequency. It is important that the rate at which the data is being written is the same to the rate at which the data is being read. Otherwise the write and read pointers would cross causing a loss of data. This is referred to as a data slip. The objective of frequency synchronization in SONET/SDH networks is to ensure that the write and read pointers operate at the same average frequency eliminating the chance of a data slip. So a systematic approach of precise frequency distribution across the entire SONET/SDH network is critical to its operation.

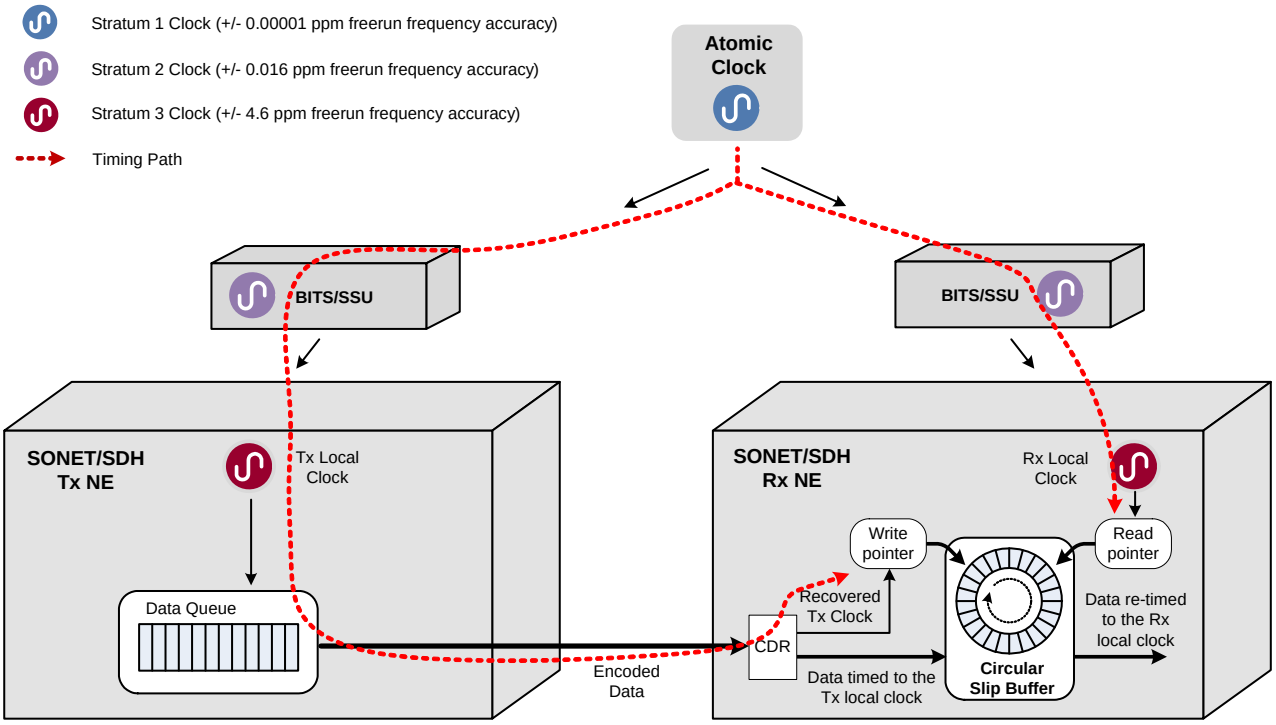


Figure 2. Data Transfer Between Two SONET/SDH Network Elements

Achieving frequency synchronization at every NE is accomplished with a hierarchical frequency distribution scheme separated into discrete categories of frequency accuracy called stratum levels. The hierarchy starts with the highest level of frequency accuracy using an atomic clock standard defined as a stratum 1 level clock with ±0.00001 ppm free run accuracy. This frequency accuracy is transmitted to the stratum 2 clocks (±0.016 ppm free run accuracy) in the building integrated timing supply (BITS), which in turn supplies all the NE's stratum 3 local clocks (±4.6 ppm free run accuracy). It is important to note that when all the clocks in the timing path are synchronized, the network element local clocks will also take on the frequency accuracy of the stratum 1 level clock. This is referred to as stratum 1 traceability and ensures no data slips.

A NE that receives its timing from a BITS source as described above is considered to be in **external timing** mode. This is the most reliable method of synchronization distribution, but it also requires the expense of maintaining redundant BITS equipment at the central office. To reduce the cost of synchronization distribution, an alternative method of synchronization distribution called **line timing** was adopted. A diagram comparing external timing and line timing methods is shown in Figure 3.

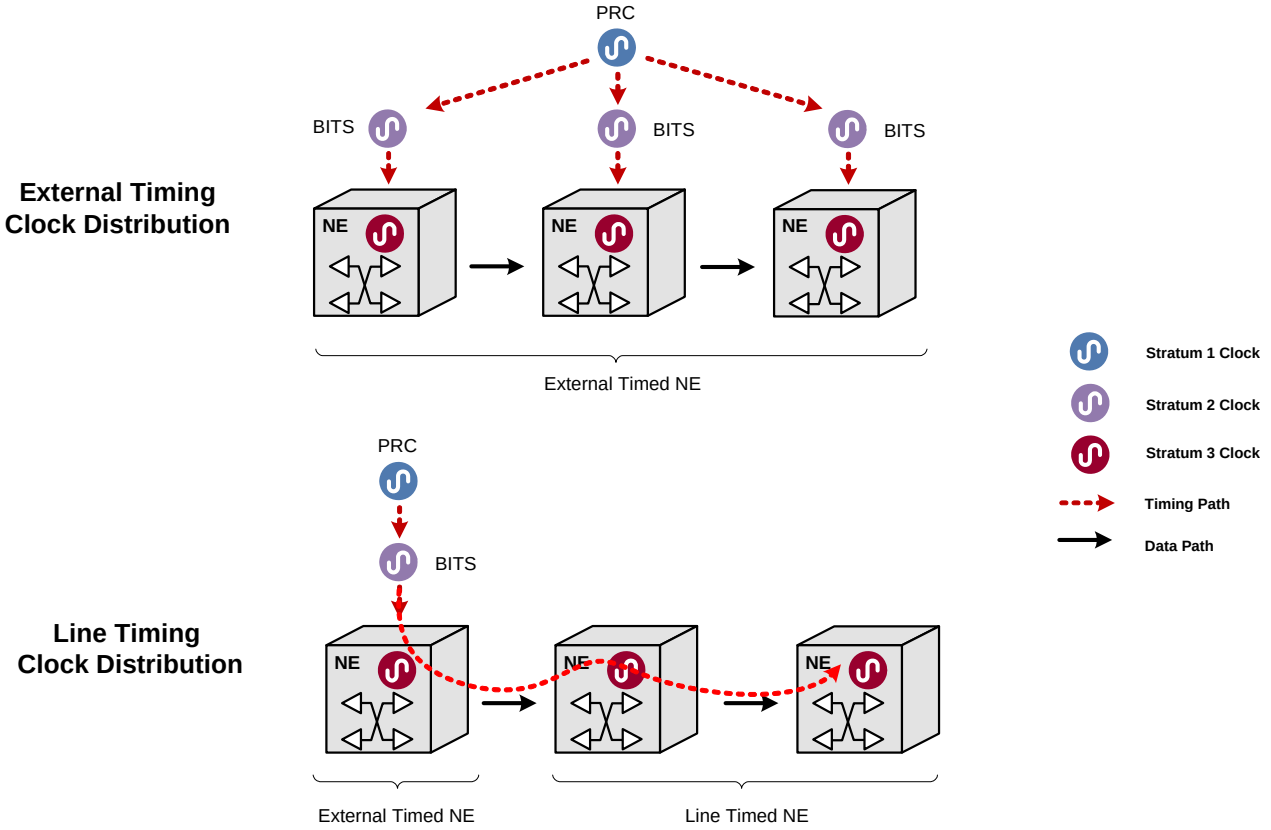


Figure 3. Line Timing Distribution in SONET/SDH Networks

Since the data transmitted from an externally timed NE is synchronized to a stratum 1 clock, the recovered clock at the receiving NE can be used as a timing source. Now that both the TX NE and RX NE are synchronized to the same source, no data slips will occur. A line timed NE can pass this stratum 1 traceable reference to downstream NEs. The concept of transmitting frequency synchronization through line timing is a very important one to understand since the same concept is used to distribute frequency synchronization across packet networks using the synchronous Ethernet (SyncE) method.

1.2. Timing In Packet Networks

Ethernet based packet networks are said to be asynchronous in nature. In other words they can reliably transfer data between two nodes with far less frequency accuracy than TDM based networks. Instead of using a circular slip buffer to resolve the frequency difference between transmitting and receiving nodes, they use a much larger data buffer at the receiver with flow control and QoS mechanisms to prevent overflow or underflow. All that is required for reliable data transmission is a free-running clock of ±100 ppm at both ends of the transmission path. This concept is illustrated in Figure 4.

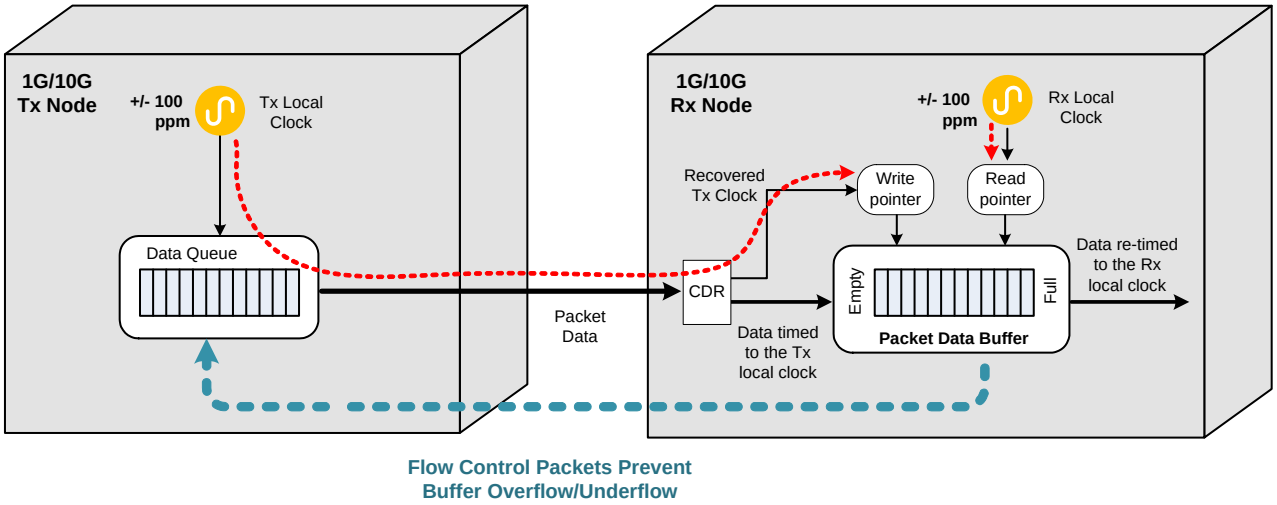


Figure 4. Data Transfer Between Two Packet Nodes

2. The Need For Synchronization Distribution in Packet Networks

Many of the services provided by packet networks operate perfectly fine with its asynchronous nature. Packet networks provide a relatively low cost means of service delivery for carriers. But some services still rely on a TDM network's ability to provide synchronized services and delivery of a highly accurate frequency and time reference. An example is wireless backhaul where precise time and frequency information is needed for proper handoff as subscribers leave a cell to enter another. As much as carriers would like the idea of managing a single network, both TDM networks and packet networks are required to deliver many of the services provided today. The challenge is ensuring proper transfer of data between synchronous and asynchronous networks. The example network in Figure 1 illustrates a core packet network combined with a SONET/SDH network that is responsible for distributing services closer to the edge. Wireless base stations provide connectivity between the network and its mobile subscribers. The issue with this network is that without frequency synchronization, the packet network cannot reliably transfer data to the TDM network. In other words, data cannot be transferred at a free-running ±100 ppm rate to a slip buffer that expects a stratum 1 traceable transfer rate (±0.0001 ppm). It would result in an unacceptable amount of data slips at the TDM interface. And without accurate frequency synchronization, the packet network would never be able to provide time and frequency information to the wireless base stations.

One possible solution to "synchronizing" the packet network is adding a BITS timing source traceable to a stratum 1 at every node that needs to communicate with a TDM network element. But this would be cost prohibitive. The ITU (International Telecommunication Union) has identified two possible solutions for distributing precise frequency synchronization across packet based networks. **Synchronous Ethernet** (SyncE) is one method and is based on physical layer clock distribution which relies on the concept of line timing as described in section 1.1. The second method relies on dedicated time stamp messages carried by data packets. The ITU does not dictate a specific timestamp protocol, but PTP (Precision Time Protocol) which was standardized by **IEEE 1588** has been universally adopted for use in timing distribution for telecom networks because of it performance. Both SyncE and packet based (1588) synchronization methods are specified by the ITU-T G.8261 standard.

2.1. Synchronous Ethernet (SyncE)

Synchronous Ethernet is a method used to distribute stratum 1 traceable frequency synchronization to packet (Ethernet) nodes that need to communicate with TDM network elements. It is also used to distribute timing to applications that rely on precise frequency synchronization such as wireless backhaul. The hypothetical network of Figure 1 has been modified in Figure 5 to show a potential SyncE timing path. Now that both packet node A and SONET/SDH network element B have frequency synchronization traceable to a stratum 1, both can communicate with each other without data slips caused by buffer overflow or underflow. This would have been impossible without frequency synchronization.

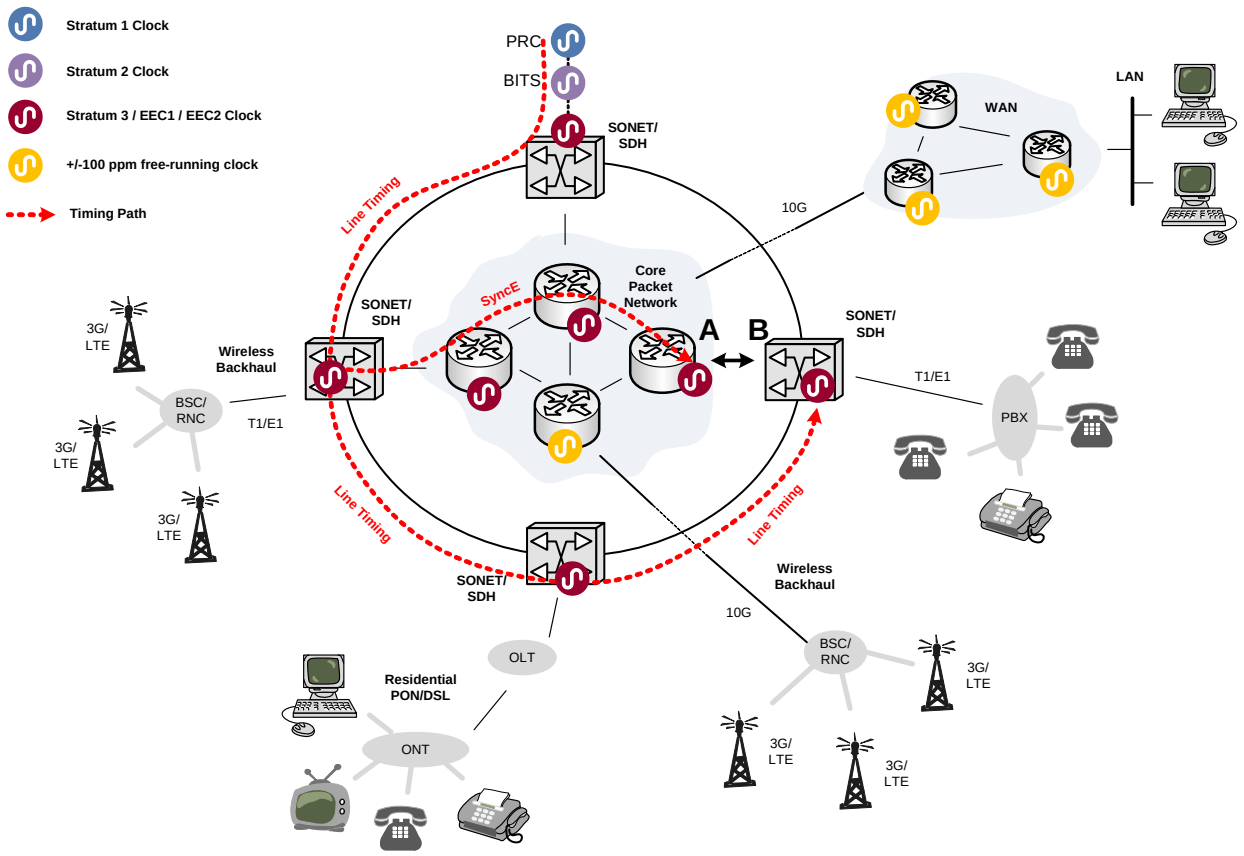
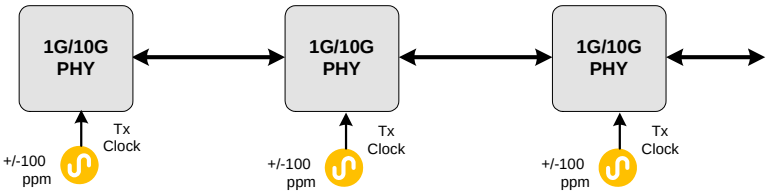


Figure 5. Synchronization Distribution of a Packet Network Using SyncE

SyncE frequency synchronization is achieved through the physical layer in the same way that SONET/SDH line timing distributes its timing. This simply means replacing the free-running ±100 ppm clocks normally supplying the TX Clocks to the Ethernet PHYs with phase-locked loops (PLL) as shown in Figure 6. A synchronization chain is formed by using a stratum 1 traceable source at one end which is then recovered at downstream PHYs and re-transmitted down the chain. It is important to note that every node in the chain must be capable of recovering and re-transmitting frequency synchronization. Inserting an asynchronous node in the path would break the chain of synchronization.

Packet Transmission using Asynchronous Timing



Packet Transmission with SyncE Physical Layer Timing Distribution

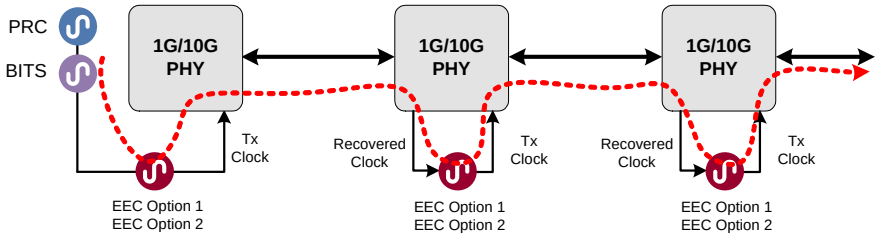


Figure 6. Distributing Synchronization Across The Ethernet Physical Layer

The performance characteristics of the PLLs used to receive and re-transmit the frequency synchronization in a SyncE chain is governed the ITU-T G.8262 standard. It defines two possible PLLs performance options: Ethernet Equipment Clock (EEC) Option 1 and EEC Option 2. EEC Option 1 is based on the 2.048 kpbs hierarchy governed by G.813 Option 1 which is used in Europe and Asia. EEC Option 2 is based on the 1.544 kpbs hierarchy governed by G.812 Type IV or Stratum 3 which is predominantly used in North America. A high level performance summary for each option is shown in Table 1. Full performance details are covered in G.8262.

Table 1. EEC Option 1 and EEC Option 2 High Level Performance Summary

	EEC Option 1 (G.813 Option 1)	EEC Option 2 (G.812 Option IV)
Free-run Accuracy (ppm)	±4.6 ppm	±4.6 ppm
Holdover Stability (ppm/day)	±2 ppm	±0.37 ppm
Filtering Bandwidth	1 - 10 Hz	0.1 Hz
Jitter Generation (ps pk-pk) (@ Ethernet Output Interface)	GbE: 400 ps pp, 2.5 kHz to 10 MHz	
	10GbE: 50 ps pp, 20 kHz to 80 MHz	

A typical application circuit of a Ethernet line card which supports SyncE is shown in Figure 7. A clock is recovered from the upstream Ethernet datapath which was transmitted using a stratum 1 traceable reference. An optional timing card provides additional wander filtering and holdover accuracy to meet the desired EEC Option level performance. Line cards located closer to the edge of the network may not require this added level of performance and can go directly into the line card PLL.

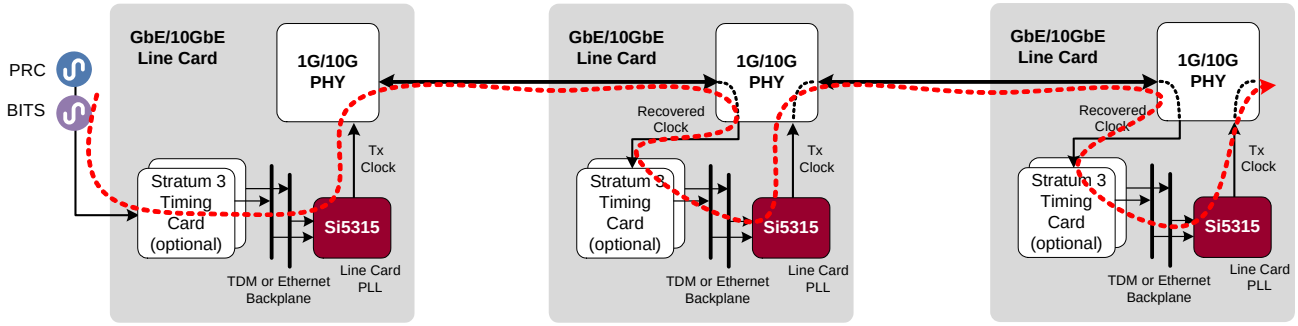


Figure 7. Application Example of SyncE Timing Distribution

The Si5315 SyncE/Telecom Jitter Attenuating Clock Multiplier is an ideal solution as a line card PLL for supplying the transmit clock to a 1G/10G Ethernet PHY supporting SyncE. It accepts TDM or Ethernet recovered clock frequencies directly from a PHY or a redundant backplane, and generates synchronous Ethernet clock frequencies that easily meet the jitter performance of both 1G and 10G Ethernet PHYs with significant margin. The Si5315's automatic hitless switching feature ensures a fully redundant system which is essential in carrier grade Ethernet equipment. The key features of the Si5315 are as follows:

- Provides jitter attenuation and frequency translation between SONET/SDH, PDH and Ethernet
- Supports ITU-T G.8262 Synchronous Ethernet equipment slave clock requirements EEC option 1. EEC option 2 supported with an optional timing card.
- Two clock inputs and two clock outputs
- Input frequency range: 8 kHz–644 MHz (e.g., TDM: 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 32.768 MHz, SONET: 19.44 MHz, 77.76 MHz, 155.52 MHz, 1G/10G/Ethernet: 25 MHz, 125 MHz, 156.25 MHz, 161.1328125 MHz, 644.53125 MHz)
- Output frequency range: 8 kHz–644 MHz (e.g., TDM: 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 32.768 MHz, 34.368 MHz, 44.736 MHz, 65.536 MHz, SONET: 19.44 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz, 1G/10G/Ethernet: 25 MHz, 125 MHz, 156.25 MHz, 161.1328125 MHz, 312.5 MHz, 644.53125 MHz)
- Very low jitter: 0.23 ps RMS (1.875–20 MHz), 0.47 ps RMS (12 kHz–20 MHz)
- Low jitter peaking: < 0.1 dB
- Simple pin control interface
- Selectable loop bandwidth for jitter attenuation: 60 to 8.4 kHz
- Loss of lock and loss of signal alarms
- Automatic/Manual hitless switching and holdover during loss of inputs clock
- Programmable output clock signal format: LVPECL, LVDS, CML or CMOS
- Single supply: 1.8, 2.5, or 3.3 V
- On-chip voltage regulator with excellent PSRR
- Small size: 6 x 6 mm, 36-QFN
- Wide temperature range: –40 to +85 ºC

2.2. Packet Based Timing (IEEE 1588)

Instead of transmitting frequency synchronization over the physical layer with line timing or SyncE methods, packet based timing relies on time stamp packets inserted in the data stream. Time stamps are inserted at the master node where a stratum 1 traceable reference is available, and then extracted at the slave clock where the synchronized frequency reference is needed. An example of a network using packet timing to distribute frequency synchronization between the master clock and its slave clocks is shown in Figure 8. The advantage of using packet based timing is that nodes between the master and slave clocks can remain asynchronous. This avoids expensive "forklift upgrades" of existing equipment. Only slave nodes that require precise frequency synchronization for communicating with other SONET/SDH network elements need to incorporate the timing extraction circuitry. The rest of the packet network can remain asynchronous. This is a key advantage over physical layer timing methods (e.g., SyncE) that need synchronous timing circuitry at every node. Another advantage of packet based timing is in its ability to transmit both frequency accuracy and phase information which is essential in applications such as wireless networks (e.g., LTE, WiMax, W-CDMA). SyncE is only capable of transmitting frequency accuracy.

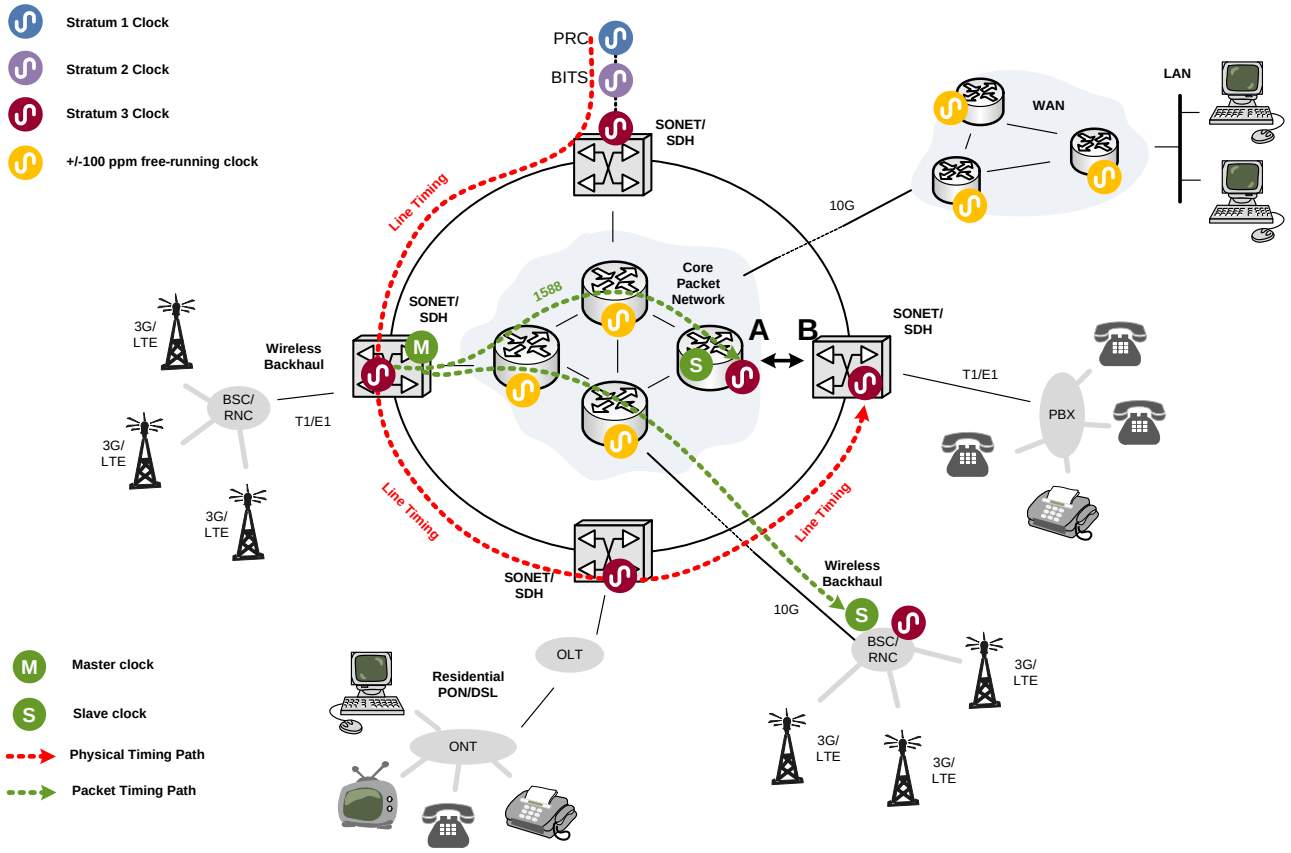


Figure 8. Packet Based Timing Distribution

A block diagram showing timing packet insertion and extraction in greater detail is shown in Figure 9. The 1588 time stamping function (which could be a stand alone device, or built-in the PHY) inserts timing packets into the data packet stream at the master clock. The stratum 1 traceable clock at the master ensures accurate frequency and phase time stamping. The combined packet stream is sent across to the slave without any adjustments made to the time stamp information by intermediate asynchronous nodes. Timing packets are extracted and processed at the slave and used to generate a clock that is synchronous with the master clock's phase and frequency.

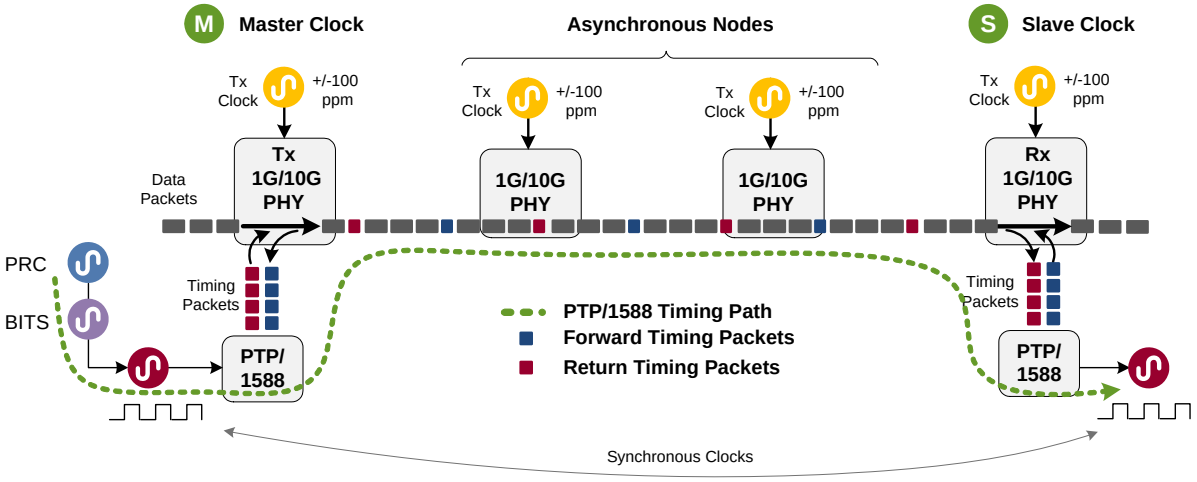


Figure 9. Timing Synchronization Using IEEE 1588

Although the distribution of frequency and phase using timestamp packets may seem like a simple concept, it faces many challenges. The 1588 protocol operates on a two way exchange of timing messages to ensure a closed feedback path, and it relies on the assumption that this two way exchange is symmetric. However this is not the case in real packet based networks. Ethernet switches and routers operate on a store and forward mechanism which introduces variable delay in receiving and transmitting packets depending on traffic patterns and congestion. This phenomena is called packet delay variation (PDV) and is the main limiting factor for the transmitted frequency accuracy and phase accuracy through the synchronous timing path. Packet delay variation worsens with the number of asynchronous nodes between the master and slave clocks, so there is a performance trade-off with adding more nodes. The IEEE 1588 protocol was recently updated with version 2 (1588v2) which introduced the concept of transparent clocking to help alleviate the performance issues introduced with PDV. With transparent clocking, time stamps are updated at every asynchronous node compensating for the variable packet delay. In other words, it makes the delay variation “transparent” to the timing distribution mechanism and ultimately improves the frequency and phase accuracy. The downside of transparent clocking is that every node in the timing path must support the new 1588v2 time stamping protocol. This will become less of an issue as new hardware is deployed in the network. Table 2 identifies the advantages for each of the packet timing distribution solutions.

Table 2. SyncE and IEEE 1588 Timing Distribution Comparison Matrix

	SyncE	IEEE 1588	IEEE 1588 + Transparent Clocking
Timing Path Continuity	All nodes in the timing path must support SyncE. Any ±100 ppm free-running nodes in the timing path will break chain of synchronization.	Only Master and Slave nodes need to support 1588. Nodes between these are totally unaware of the timing packets and can run using ±100 ppm free-running clocks.	All nodes between Master and Slave need to support 1588. Nodes between these can run using ±100 ppm free-running clocks.
Number of Nodes in the Synchronous Timing Path	Frequency accuracy can be distributed over several nodes (<60) before being re-timed by a higher level clock.	Number of ±100 ppm free-running nodes in the timing path between the master and slave is limited (<10)	Number of ±100 ppm free-running nodes in the timing path between the master and slave is improved (>10). The maximum limit is dependant on the application and the loop algorithms.
Frequency Accuracy	Meets the same performance requirements as SONET/SDH line timing.	Much lower frequency accuracy than SyncE. Performance is dependent on the network's PDV.	Lower frequency accuracy than SyncE. Performance is much less dependent on the network's PDV.
Phase Alignment	Not supported	Phase alignment up to 1 µs is possible depending on PDV.	Phase alignment much less than 1 µs is possible.
Time Of Day	Not supported	Supported	Supported

A typical implementation example of packet timing distribution is shown in Figure 10. Timing packets are recovered from the receive PHY at the slave clock, and interpreted at the 1588 core. A CPU retrieves the extracted 1588 timestamps, processes the information using a control loop algorithm, and steers a digitally controlled crystal oscillator to produce the final synchronous clock which is traceable to the master clock.

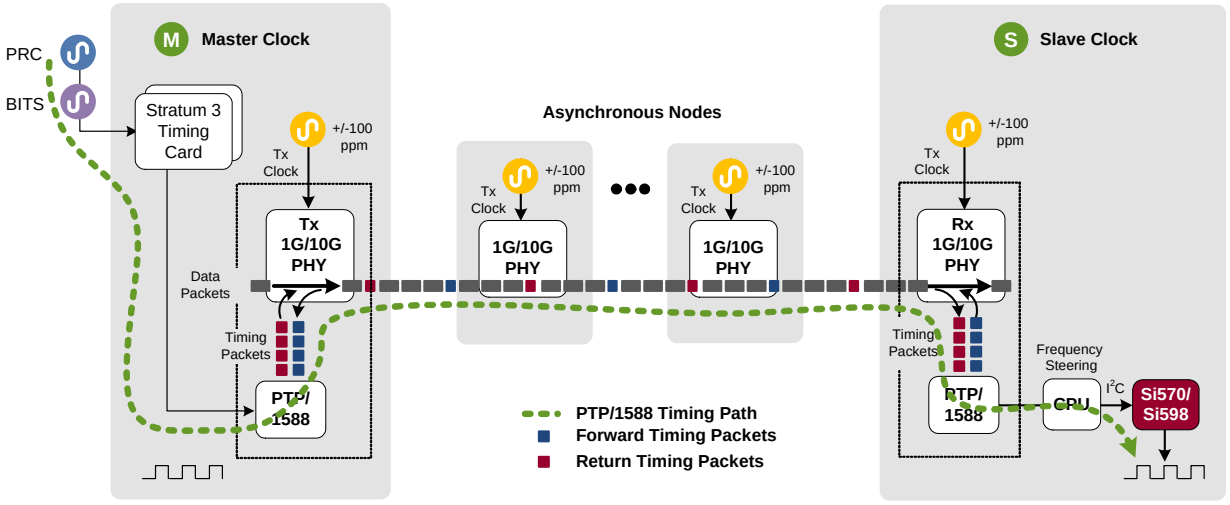


Figure 10. Application Example of 1588 Timing Recovery Using the Si570/Si598

The Si570 I^2C programmable crystal oscillator offers digitally controlled frequency adjustment which is necessary for converting 1588 timestamp information to a final output clock. The device's excellent jitter performance of 0.4 ps RMS allows it to supply 10G PHY transmit clocks without any further jitter attenuation. Alternatively, the Si598 I^2C programmable crystal oscillator can be used for applications with less demanding performance requirements. Table 3 list some key performance parameters for each of these oscillators.

Table 3. Si570/Si598 I^2C Programmable Crystal Oscillator Features

	Si570	Si598
Center Frequency (programmable)	10 MHz–1.4 GHz	10–810 MHz
Frequency Adjustment Resolution	0.090 ppb (min), 3500 ppm (max)	0.028 ppb (min), 3500 ppm (max)
RMS Jitter (12 kHz–20 MHz)	0.38 ps (typ), 0.50 ps (max)	0.50 ps (typ), 1.0 ps (max)
Temperature Stability	±7 ppm	±20 ppm
Note: ppb = part per billion, ppm = part per million		

In some applications it makes sense to transmit both SyncE and timing packets to take advantage of SyncE's excellent frequency accuracy and 1588's phase accuracy and time of day capability. The example in Figure 11 shows timing distribution using both a SyncE path and a 1588 timing path. The master clock which is traceable to a stratum 1 generates both the SyncE reference and the 1588 time stamp packets. Intermediate nodes recover and propagate the SyncE physical layer timing using the Si5315 as seen in previous examples. Depending on the application and where the SyncE nodes are located in the network, an optional Stratum-3 timing card may be used in combination with the Si5315 to provide additional wander filtering and holdover capabilities. Timing packets generated by the master clock are also propagated through the datapath of the intermediate nodes. At the slave clock, both the SyncE clock and 1588 packets are recovered. The Si5326 Any-Frequency Clock Multiplier/Jitter Attenuator provides the final clock generation point which can synchronize to either the SyncE or 1588 timing paths. In SyncE mode, the Si5326 locks to the recovered clock(s) directly from the 1G/10G PHY or from the optional stratum 3 timing card(s) if required by the application. In 1588 mode, the Si5326 uses its holdover mode to allow the 1588 synchronous output of the Si570 to steer its output frequency through the reference input (XA/XB). The key features of the Si5326 are as follows:

- I^2C or SPI programmable
- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 0.3 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Dual clock inputs with manual or automatically controlled hitless switching
- Wide pull-in and lock-in range (> 500 ppm)
- Dual clock outputs with selectable signal format
- LOL, LOS, FOS alarm outputs
- Digitally-controlled output phase adjustment
- Small size: 6 x 6 mm 36-lead QFN

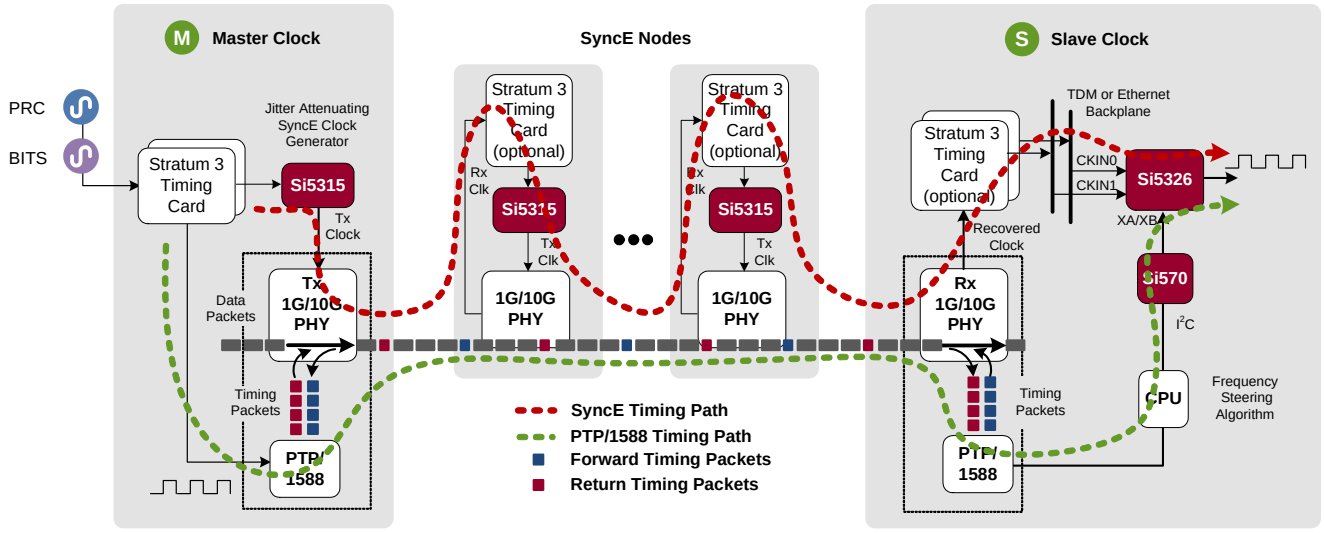


Figure 11. Application Example of SyncE and 1588 Timing Recovery Using the Si5326

3. Conclusion

There is an undeniable need to combine services supplied by data efficient packet networks with the ones served by the large installed base of traditional SONET/SDH networks. Without synchronization, SONET/SDH services cannot operate over these asynchronous packet networks. Both SyncE and packet timing/1588 offer viable solutions in unifying service delivery over both networks. Silicon Labs provides key timing components to enable timing distribution over these next generation networks.

4. References

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DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated Figure 10.

NOTES:

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