Application Note AN-1087

Design of Secondary Side Rectification using IR1167 SmartRectifier™ Control IC

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Table of Contents

Device Overview

SmartRectifier™ Concept

Operation and analysis in CCM & DCM Flyback

Operation in Resonant Converters

Typical System Schematics and Passive Components Nomenclature

Design Procedure & example

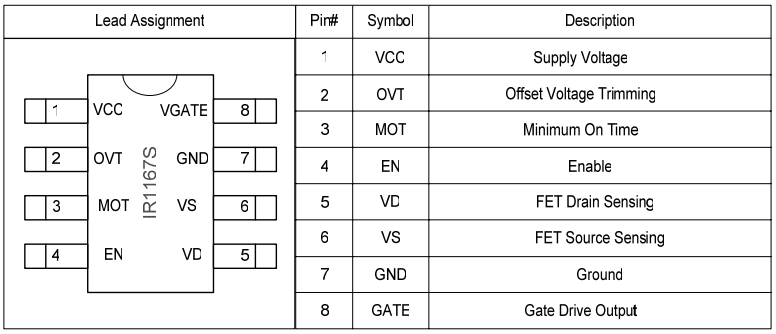
PCB Layout Guidelines

Symbols list

Introduction

IR1167S is a smart secondary-side driver IC designed to drive N-Channel power MOSFETs used as synchronous rectifiers in isolated Flyback converters. The IC can control one or more paralleled MOSFETs to emulate the behavior of Schottky diode rectifiers.

The drain to source voltage of the MOSFET is sensed differentially to determine the level of the current and the device is turned on and off in close proximity of the zero current transition. The pinout for the 8 pin device is shown below.



Pin#	Symbol	Description
1	VCC	Supply Voltage
2	OVT	Offset Voltage Trimming
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing
7	GND	Ground
8	GATE	Gate Drive Output

Figure 1: IR1167 SmartRectifier™ control IC pin assignment.

SmartRectifier™ Concept

The typical power stage schematic for a flyback converter with synchronous rectification (low-side configuration) at the output is shown below.

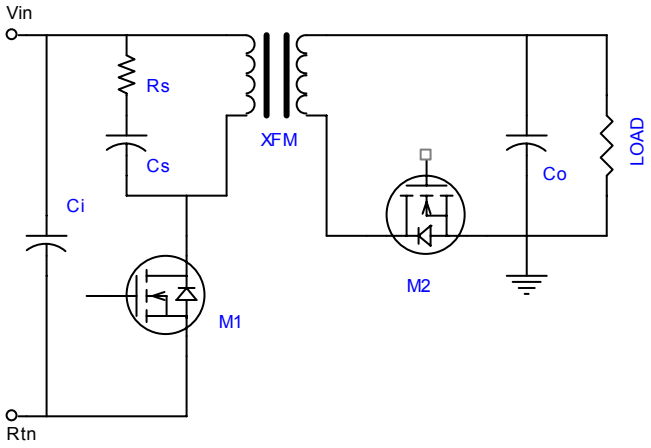


Figure 2: Typical schematic of a flyback converter with synchronous rectification.

When the primary device M1 is turned off, the secondary current will flow through the body diode of the MOSFET M2 (which is analogous to the current flowing through the output diode when diode rectification is used).

The SmartRectifier™ Control Technique is based on sensing the voltage across the MOSFET and comparing it with two negative thresholds to determine the turn on and off transition for the device. A higher negative threshold, V_{TH2}, detects current through the body diode and hence, controls the turn on transition for the power device. Similarly, a second externally programmable smaller negative threshold, V_{TH1}, determines the level of the current at which the device turns off.

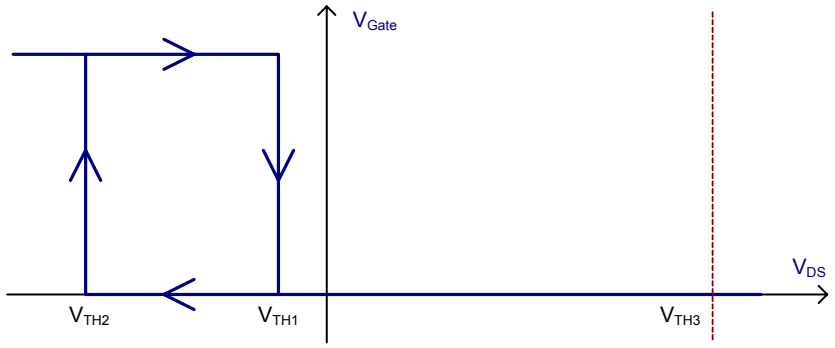


Figure 3: IR1167 SmartRectifier™ control IC differential voltage sensing thresholds.

Additional control logic has been incorporated to prevent false turn off and gate chattering when the device current transitions between its body diode and channel.

When the power device is turned on, the instantaneous sensed voltage reduces to $R_{DSon} \cdot I_D$ and depending on the level of the device current, could fall below the turn off threshold and cause false device turn off. Additionally, the device turn on is also associated with some parasitic ringing between the transformer leakage inductance and device output capacitance.

Operation and analysis in CCM & DCM Flyback

The IR1167 SmartRectifier™ IC can emulate the operation of diode rectifier by properly driving a Synchronous Rectifier (SR) MOSFET. The rectifier current is sensed by the input comparator using the power MOSFET R_{DSon} as a shunt resistance and the GATE pin of the MOSFET is driven accordingly depending on the level of the sensed voltage with respect to the 3 thresholds shown in Figure 3. Internal blanking logic is used to prevent spurious transitions and guarantee operation in continuous (CCM), discontinuous (DCM) and critical (CrCM) conduction mode.

The modes of operation for a Flyback circuit differ mainly for the turn-off phase of the SR switch, while the turn-on phase of the secondary switch (which correspond to the turn off of the primary side switch) is identical.

➢ *Turn On Phase*

When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative V_{DS} voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold V_{TH2}. At that point, the IR1167 will drive the gate of MOSFET on which will in turn cause the conduction voltage V_{DS} to drop down.

This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off; hence, an externally programmable Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.

The programmed MOT will limit also the minimum duty cycle of the SR MOSFET and, as a consequence, the max duty cycle of the primary side switch.

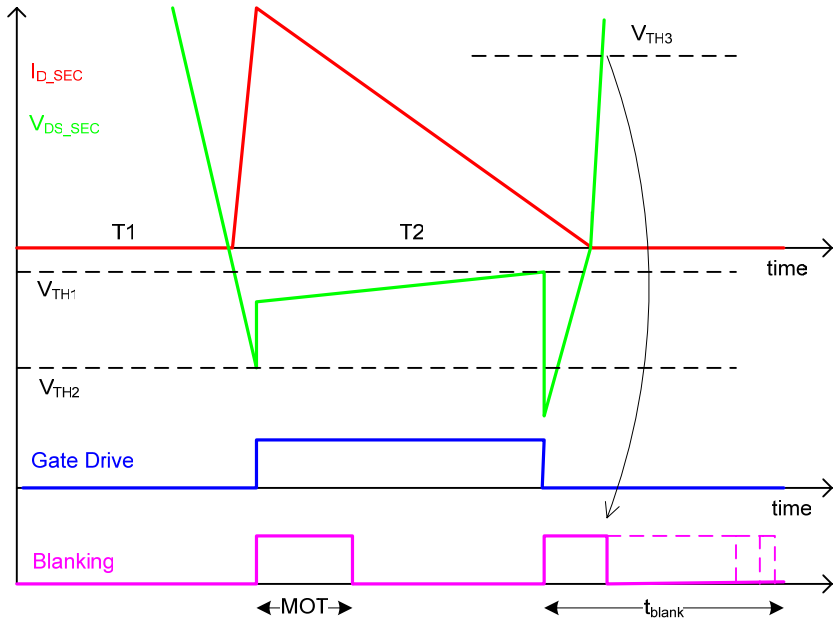


Figure 4: MOT and t_{BLANK} during operation in DCM.

Notice both Minimum On Time and Blanking time logic are allowed only once per switching cycle; it is necessary that V_{DS} reaches V_{TH3} (therefore primary turn on) for them being enabled again (therefore ready for the next switching cycle).

➢ *DCM/CrCM Turn Off Phase*

Once the SR MOSFET has been turned on, it will remain on until the rectified current will decay to the level where V_{DS} will cross the turn-off threshold V_{TH1}. This will happen differently depending on the mode of operation.

In DCM the current will cross the threshold with a relatively low $\frac{dI}{dt}$. Once the threshold is crossed, the current will once again flow through the body diode, causing the V_{DS} voltage to jump negative. Depending on the amount of residual current, V_{DS} may again trigger the turn on threshold: for this reason V_{TH2} is blanked for an internally set blank time t_{blank} (as shown in Figure 4) after V_{TH1} has triggered. As soon as V_{DS} crosses the positive threshold V_{TH3}, this blanking time is terminated and the IC is ready for next conduction cycle.

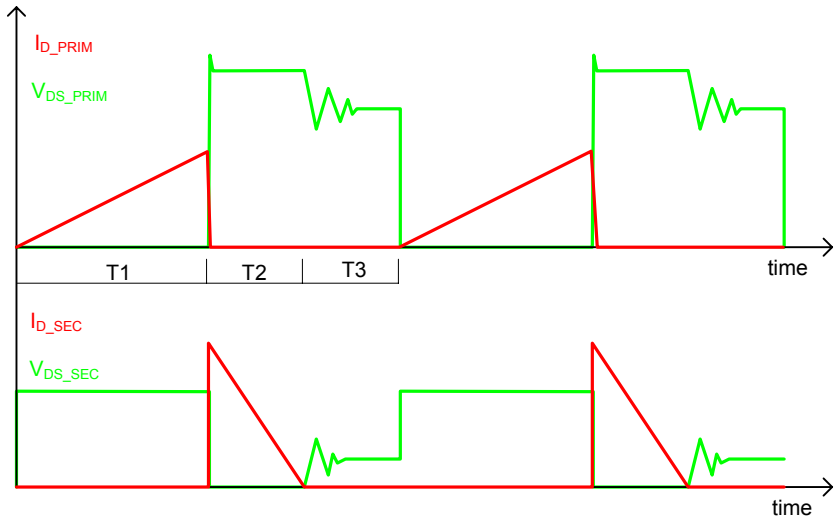


Figure 5: DCM operating flyback converter simplified waveforms.

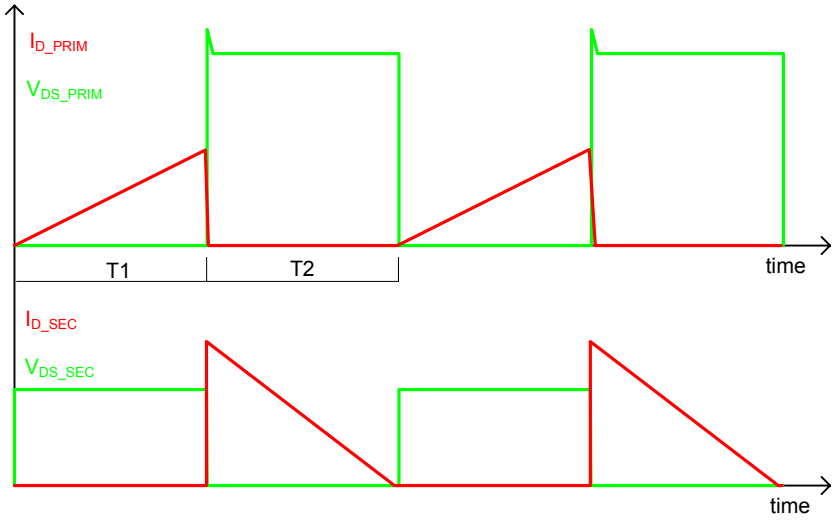


Figure 6: CrCM operating flyback converter simplified waveforms.

➢ *CCM Turn Off Phase*

During the SR FET conduction phase the current will decay linearly, and so will V_{DS} on the SR FET. Once the primary switch will start to turn back on, the SR FET current will rapidly decrease crossing V_{TH1} and turning the gate off. The turn off speed is more critical here to avoid cross conduction on the primary side and reduce switching losses. The blanking period is also applied in this case, but given the very fast nature of this transition, it will be reset as soon as V_{DS} crosses V_{TH3}.

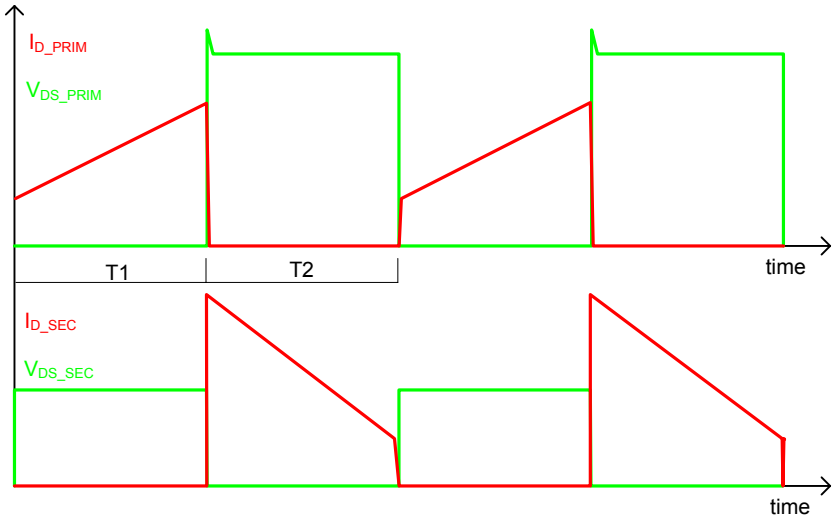


Figure 7: CCM operating flyback converter simplified waveforms.

Operation in Resonant Converters

Figure 8 shows the typical secondary-side schematic for a series resonant converter with a capacitive output filter. Implementing synchronous rectification in such applications would require 2 current sense transformers, 2 high speed comparators and finally 2 high current, low propagation delay gate drivers needed to drive the two power devices. Existing monolithic solutions are based on PLL control techniques and rely on synchronizing signals from the primary-side to anticipate the turn off transition for the secondary MOSFETs; hence, they cannot guarantee reliable operation when the converter operates in burst mode during light and no load conditions. The SmartRectifier™ control technique operates completely independent of the primary-side switching technique and the low $\frac{dI}{dt}$ transitions in the resonant converter make the IR1167 an excellent candidate in such applications. Figure 9 illustrates this with waveforms.

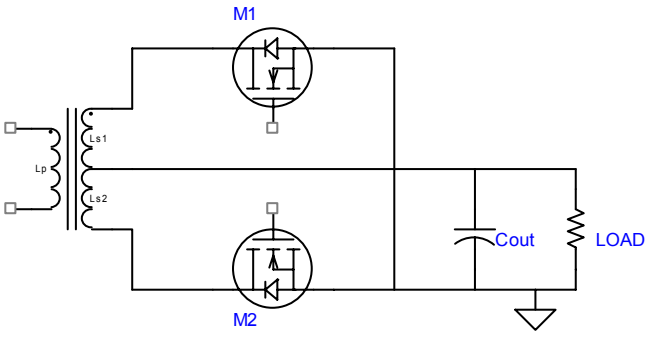


Figure 8: Series resonant converter secondary-side general schematic.

IR1167 operates completely independent of the primary-side switching technique and the low $\frac{dI}{dt}$ transitions make it an excellent candidate for such applications as shown in Figure 9 below.

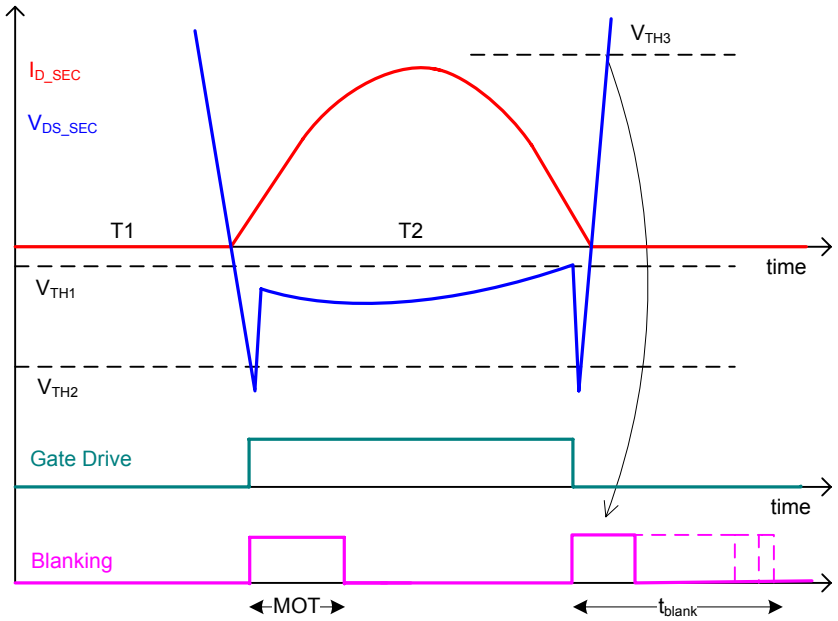


Figure 9: Series resonant converter with IR1167 SmartRectifier™ control IC general waveforms.

In resonant converter applications, output voltage regulation can be achieved by operating in fixed or variable frequency (50% duty cycle) operating modes. In variable frequency applications, the converter operates at the minimum switching frequency at low line-full load conditions and at the maximum frequency at high line-no load conditions.

Hence, the MOT selection for resonant converters can simply be based on the maximum switching frequency of the converter. MOT ensures proper gating signals for the synchronous MOSFETs during light load conditions (i.e. operating at maximum switching frequency), and the situation only improves when the converter operates at heavier loads.

Typical System Schematics and Passive Components Nomenclature

Passive components needed for IR1167 operations are:

- C: supply decoupling capacitor
- R_g: synchronous MOSFET gate resistor
- R_{MOT}: Minimum On Time setting resistor

Component not necessary but recommended:

- R_{CC}: series resistor on supply

In all the low side configurations, power can be drawn directly from converters' output whenever its regulated voltage falls in the recommended range (12-20V). In all other cases, recommendation is to provide a dedicated supply through:

- Auxiliary transformer winding if high side
- Transformer main winding tap if low side

Figure 10 to Figure 16 show typical systems schematics.

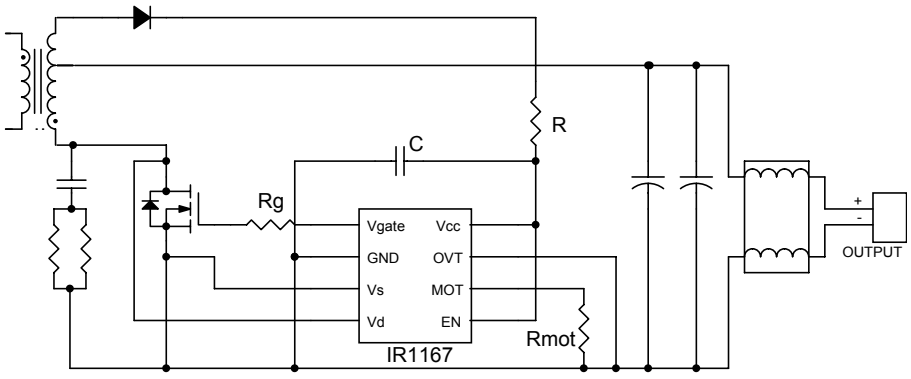


Figure 10: single ended, low side rectification, supply from winding tap (V_{output} < 12V).

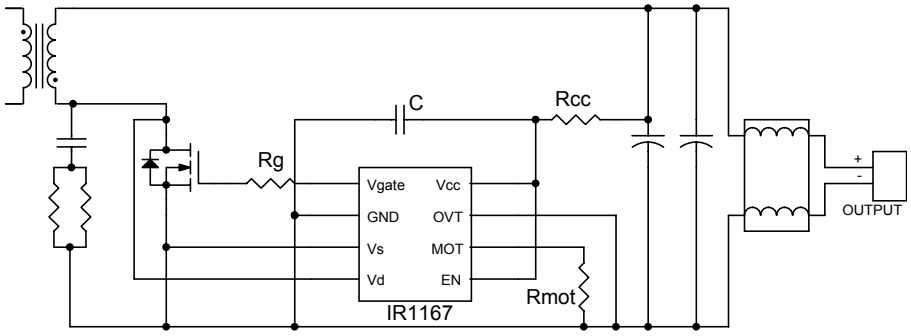


Figure 11: single ended, low side rectification, supply from output voltage (V_{output} = 12-20V).

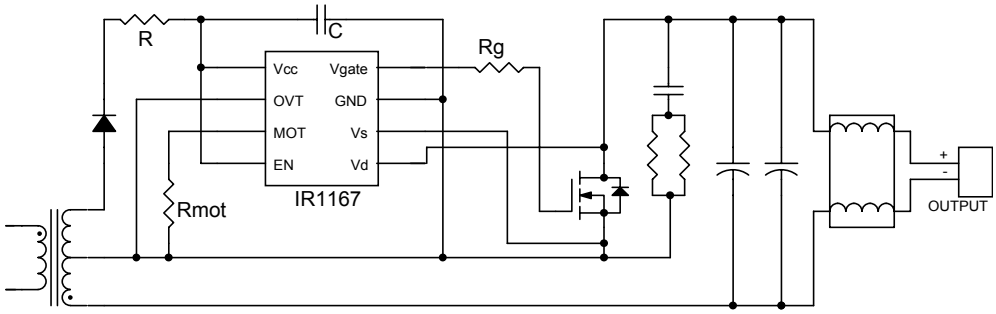


Figure 12: Single ended, high side rectification, supply through aux winding (output voltage independent).

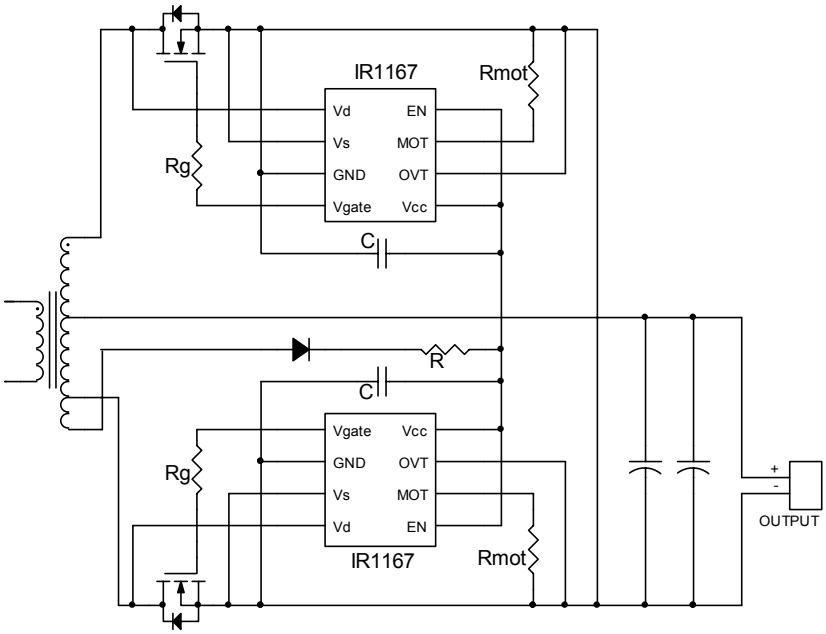


Figure 13: Center tap, low side rectification (Half or Full bridge resonant), supply from extra winding (V_{output} < 6V).

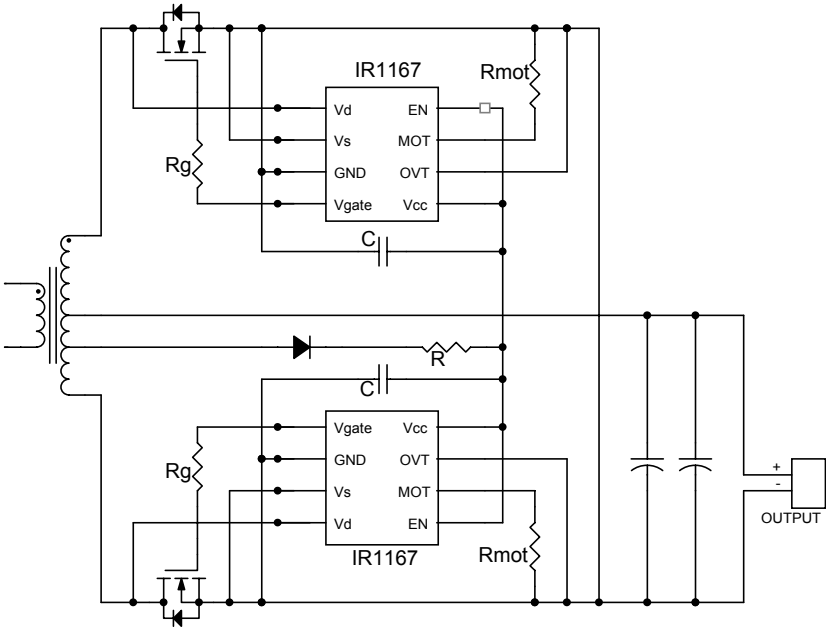


Figure 14: Center tap, low side rectification (Half or Full bridge resonant), supply from winding tap (6V < V_{output} < 10V).

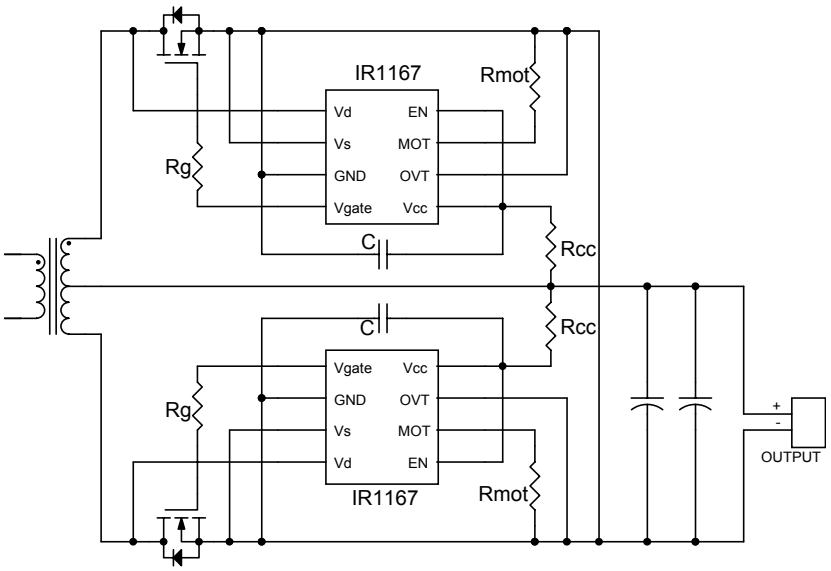


Figure 15: Center tap, low side rectification (Half or Full bridge resonant), supply from output voltage (V_{output} = 12-20V).

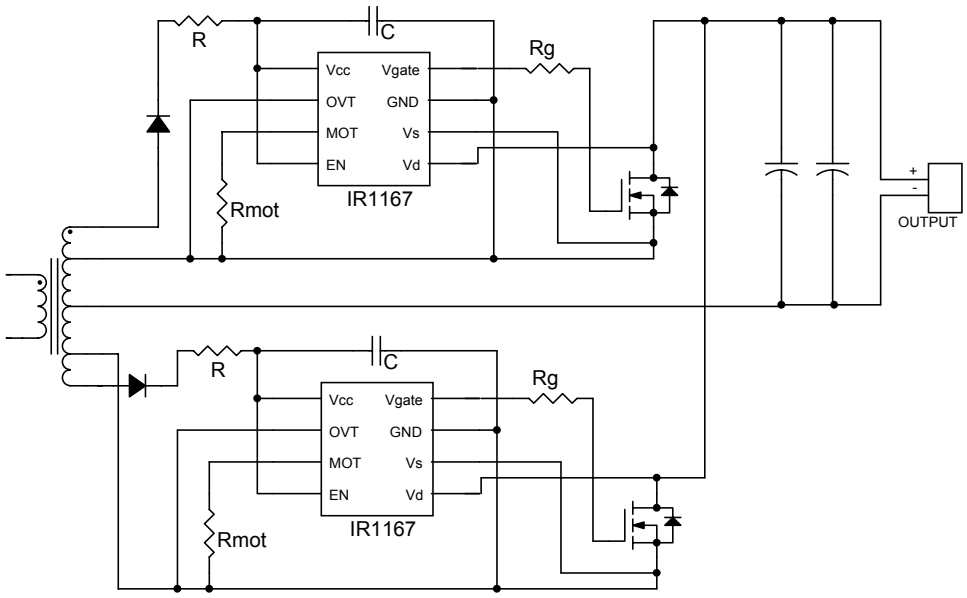


Figure 16: Center tap, high side rectification (Half or Full bridge resonant), supply from extra winding (output voltage independent).

Required System Parameters

Fundamental values to be captured on the system if not known by design are

1. maximum switching frequency $f_{SW_{\max}}$ and minimum operating switching frequency $f_{SW_{\min}}$
2. secondary minimum conduction time, also called (in SmartRectifier™ terminology) Minimum On Time (MOT)
3. mode of operations: Continuous (CCM), Discontinuous (DCM) or Critical (CrCM) conduction mode of operations
4. The maximum temperature of the environment in which the IR1167S IC will operate, $T_{IC_{amb}}$ (this is normally the maximum PCB temperature)
5. The available supply voltage V_{supply}. It can be the converter output voltage (for low side rectification systems) or a dedicated supply (i.e.: transformer extra winding or tap)

➢ *Minimum On Time (MOT) Determination*

In order to properly capture the minimum on time on an existing system, the following procedure is recommended. First, probe the output rectifier voltage (or current) and set the oscilloscope in order to trigger the conduction waveform. Second, identify the condition (AC main line and load) which visually shows reducing the conduction waveform at minimum (normally small or no load, high line). Then, using measuring tools, monitor the conduction pulse width statistically. Most equipments include that function. Due to variable frequency nature of most flyback controllers, width of that pulse can vary significantly. Target is therefore to capture the lowest possible value while slightly varying both, load and main line, around the identified working point (if the condition is at no load, there is no need to apply some load).

Figure 17 shows the acquired statistic -

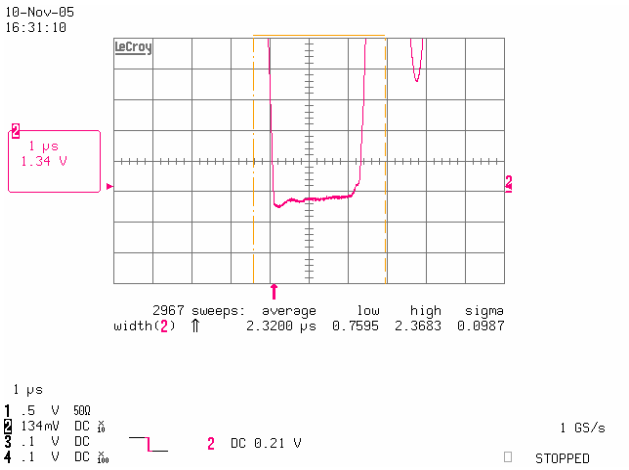


Figure 17: Minimum On Time determination on an existing system.

Notice that the minimum value (low) showed in the scope statistic could easily mislead. It can be due to several reasons not directly linked to reality (trigger issues, measuring issues, etc.) and it's normally the minimum absolute recorded. In this case, the recommendation is to properly use the statistical data, assuming the average minus 6 times the standard deviation reasonably represents the minimum possible value (3ppm). In the present example

$$MOT = 2.32 - 6 \cdot 0.0987 = 1.73 \mu s$$

➢ *Maximum Switching Frequency Determination*

Like in MOT determination, also max frequency can be variously located around different power supply working conditions. A simple sweep of AC line and load can easily show around which working point this condition occurs. Then using statistical tool, max frequency is easily measured around the identified working point (slight variation of load and main AC line).

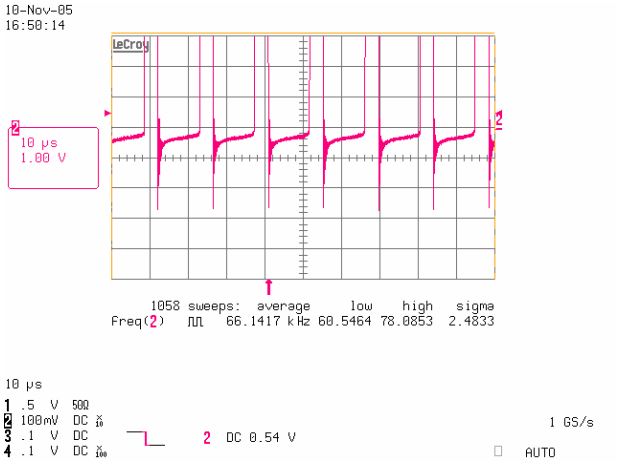


Figure 18: maximum switching frequency determination on an existing system.

Also in this case, low and high value shown on scope could easily misled. Having this parameter thermal impact on IR1167 design only and being this averaged in nature (see electrical procedure), we recommend keeping average plus 3 sigma (0.3%) as a good rule for determining the maximum switching frequency. In the present example:

$$f_{SW_{\max}} = 66.14 + 3 \cdot 2.48 = 73.6kHz$$

➢ *Mode of Operation Determination*

Mode of operation can be easily checked sweeping both, AC main line and load across their range.

Detailed Design Procedure

Following procedure assumes the synchronous MOSFET has been already identified as well as the above mentioned systems parameters

a. OVT setting

Table 1 shows the guidelines in properly choosing the right OVT (turn on and off comparator Offset Voltage Trimming) threshold.

System mode of operation	OVT connected to (typical values)
DCM or CrCM	Ground, V_{TH1}= -3.5mV
Boundary CCM	Floating, V_{TH1}= -10.5mV
CCM	V_{CC}, V_{TH1}= -19mV

Table 1: OVT setting guideline as function of system mode of operations

The basic idea behind this is the need to ideally approximate a rectifier behavior, having the voltage sense as a sole input to the controller. In DCM or CrCM, it is obvious the use of the comparator threshold closer to zero, in order to maximize the conduction through the MOSFET channel.

In CCM conditions, the reverse voltage normally appears quickly across the rectifier, requiring the controller to turn it off with the minimum possible delay. The two lower comparator thresholds enable earlier detection of current fall. Ideally, the optimized system would have one of those two thresholds as closest as possible to the MOSFET V_{DS} at the end of the conduction cycle as shown in Figure 19.

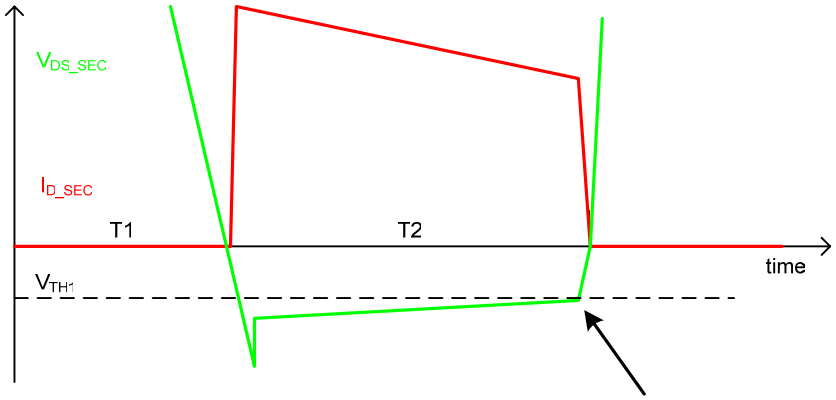


Figure 19: OVT design for CCM operations.

Further requirements for CCM operations are explained at the end of this design procedure.

In boundary CCM (CCM during ac main or load boundary conditions only, therefore rarely occurring in normal system operating conditions) the floating OVT threshold generally represents a good compromise.

b. IC current consumption calculation

First, from selected synchronous MOSFET total gate charge Q_g and gate to drain charge Q_{gd} data have to be identified, together with the corresponding gate voltage V_{gs}. Because of the IR1167 mode of operations, secondary current initially flows through the body diode, therefore the turn on gate characteristic doesn't include the Miller charge. Figure 20 shows how a regular gate characteristic (black continuous line) changes when the switch is turned on at zero or slightly negative drain to source voltage (red discontinuous line)

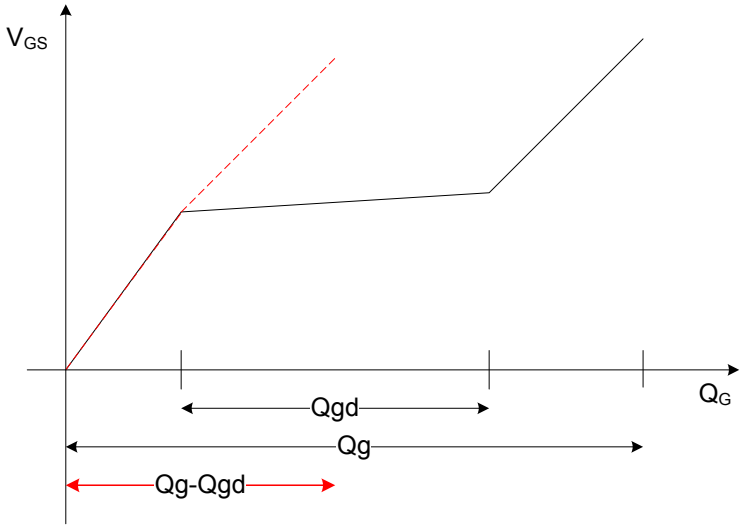


Figure 20: MOSFET gate characteristic when driven by SmartRectifier™ control IC.

It is evident much less charge is required and the behavior can satisfactorily be modeled as a capacitor:

$$C_{sync} = \frac{Q_g - Q_{gd}}{V_{gs}}$$

If more parts are paralleled, the above capacitance have to be multiplied for the number of devices.
The maximum IC required current can then be calculated as following:

$$I_{CC} = f_{SW_{\max}} C_{sync} V_{g_{high}} + \left(I_{QCC} + 7 \cdot 10^{-9} f_{SW_{\max}}\right)$$

where $V_{g_{high}}$ is the IR1167 gate driver output voltage and f_{SW_max} is the converter maximum switching frequency as previously identified. The first term is entirely due to synchronous MOSFET gate drive while the second term accounts for the IC internal logic consumption in regular operations (the factor $7 \cdot 10^{-9}$ accounts the frequency dependent current requirements for the internal logic).
Notice this term is independent from V_{CC} voltage.

c. Gate and supply series resistors design and thermal verification

IR1167S based synchronous rectification has the prerogative to turn the switch on and off at V_{DS} levels close to zero. The gate resistor hasn't therefore impact on transitions and can be designed on a different basis.

In order for the gate loop to be optimized, oscillations have to be avoided in regular operations. Assuming the total gate trace loop inductance is known (a very first estimation can be 1nH/mm of physical trace length), the minimum recommended gate resistor will be

$$R_{g_{loop}} > 2\sqrt{\frac{L_g}{C_{iss}}}$$

Where C_{iss} is the switch input capacitance (from switch datasheet).

Figure 21 shows how this critical resistance value varies with the overall gate loop inductance for some popular International Rectifier MOSFETs.

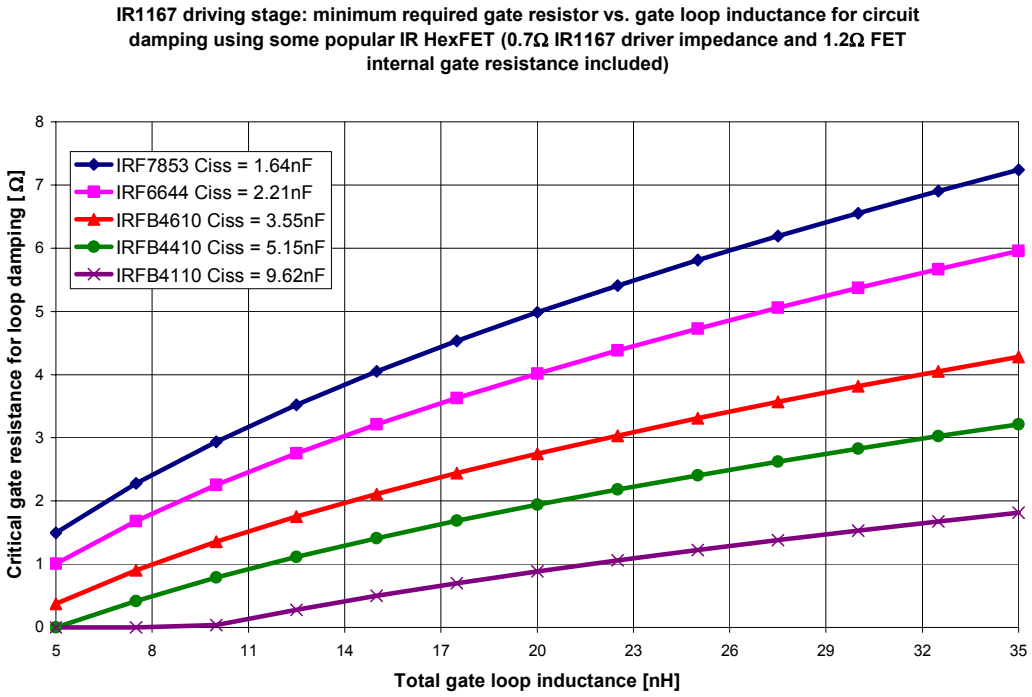


Figure 21: minimum external gate resistor vs. gate loop inductance for some MOSFETs.

It is evident how a good layout practice can dramatically reduce this requirement.

Now, let's consider the well known series RC network transient: the energy dissipated by the resistor is exactly equal to the energy stored in the capacitor. IR1167S internal gate driver is of course always in series with the external gate resistor, which means they will linearly share the power dissipation.

First, let's calculate the energy stored in the MOSFET gate:

$$E_g = \frac{1}{2} C_{sync} V_{g_{high}}^2$$

The power dissipated by the driver buffer AND the total gate resistance will therefore be

$$P_{dr} = 2 f_{SW\max} E_g$$

The driver buffer and the total gate resistance will linearly share this power dissipation as described in the following relationship:

$$P_{R_g} = \left(\frac{R_g}{R_g + R_{Source}} + \frac{R_g}{R_g + R_{Sink}} \right) \cdot \frac{P_{dr}}{2}$$

Rearranging this last relationship

$$\frac{P_{R_g}}{P_{dr}} = \frac{1}{2} \left(\frac{R_g}{R_g + R_{Source}} + \frac{R_g}{R_g + R_{Sink}} \right)$$

and solving it with respect to R_g (which includes the external gate resistor and the MOSFET internal gate resistance), it is possible to plot the percentage of the total driving power dissipated into the gate resistor as a function of its value. This is also useful for proper dimension the gate resistor itself. Notice on IR1167S datasheet, pull up and pull down resistances are defined; while $R_{Sink} = r_{down}$, $R_{Source} = 1.1 r_{up}$ in order to account for some extra energy dissipated for voltage clamping.

IR1167 driving stage: percentage of the required driving power P_{dr} dissipated in the gate resistor as a function of the gate resistor value

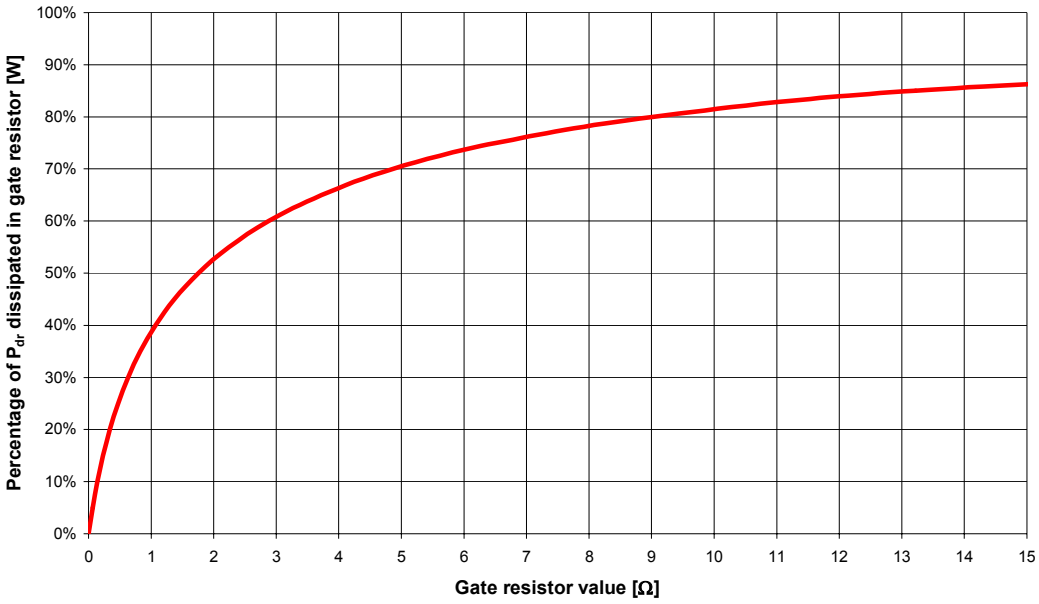


Figure 22: percentage of gate driver power dissipated in the gate resistor as function of its value.

It is evident the asymptotic nature of the curve (it would require an infinite gate resistor for dissipating all the power in it).

The final step is the thermal verification for the chosen value. Using the maximum thermal resistance junction to ambient, the maximum temperature (where ambient refers to the environment in which the IC will work , i.e. box, PCB etc.) and the IC maximum junction temperature, it is now possible to calculate the maximum allowable IC power dissipation

$$P_{IC_{\max}} = \frac{T_{J\max} - T_{IC\_amb}}{R_{\vartheta JA}}$$

where, according to IR1167 datasheet, $R_{\theta JA}$=128°C/W.

Because P_{Rg} is known and supply current has already been calculated, this will imply to limit the V_{CC} supply voltage (therefore the maximum input power for IR1167)

$$V_{CC_{\max}} = \frac{P_{IC_{\max}} + P_{R_g}}{I_{CC}}$$

Figure 23 shows maximum allowable IR1167A V_{CC} vs. maximum switching frequency for some popular International Rectifier 100V MOSFET, assuming 1Ω external gate resistor and 85ºC environment

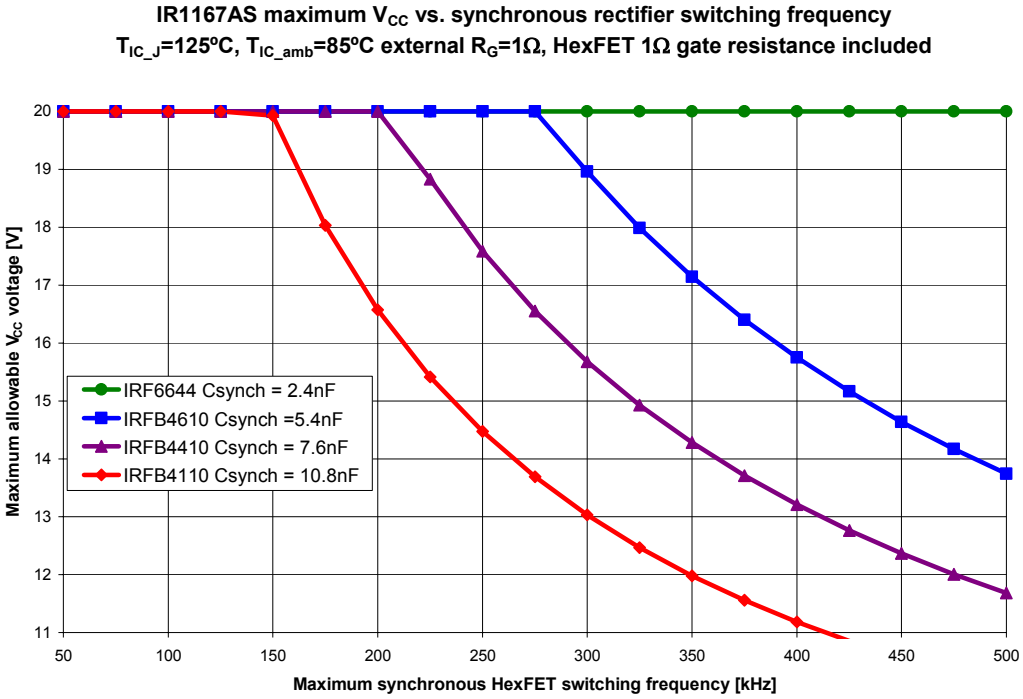


Figure 23: Max V_{CC} supply voltage vs. switching frequency for some chosen MOSFET, IR1167AS IC ΔT_J=40ºC.

In order to avoid UVLO issues, V_{CC} designs below 12V should be avoided.

It is clear how supply voltage and gate resistor play a major role in the design trade off. In most commercial systems, the minimum gate resistor value for loop damping will satisfy the thermal requirements.

If not, the procedure has to be iterated taking the following steps

Step 1: decrease the V_{CC} to the lowest possible value through a series resistor:

$$R_{CC} = \frac{V_{supply} - V_{CC}}{I_{CC}}$$

If this allows V_{CC} to comply the thermal limit, then gate resistor value can be kept as designed.

It is worth mentioning the additional benefit of adding some series resistance to supply: an enhanced filtering effect with local decoupling capacitor. For systems powered from the output (no dedicated power through windings, etc.) this can result in smoother operations

Step 2: increase the gate resistor value. This can be of some effect if a small resistance has been used, according to Figure 22.

d. Decoupling capacitor

Several techniques are possible for decoupling capacitor sizing, depending upon system topology and or special requirements. As general guideline a capacitor of at least 100nF should be used.

The two most common cases are IR1167S powered directly form the output or from a dedicated winding.

In the first case, in order to reduce the voltage ripple and possible noise, a good criteria is to use a series resistor on supply (if not already used for thermal management reasons) and size the capacitor in order to obtain a low pass filter with pole frequency a couple of octaves below the minimum operating switching frequency (not stand-by)

$$C_{\min} = \frac{2}{\pi \cdot f_{SW_{\min}} \cdot R_{CC}}$$

Figure 24 chart shows some obtained values as examples. A minimum value of 100nF limits the curves.

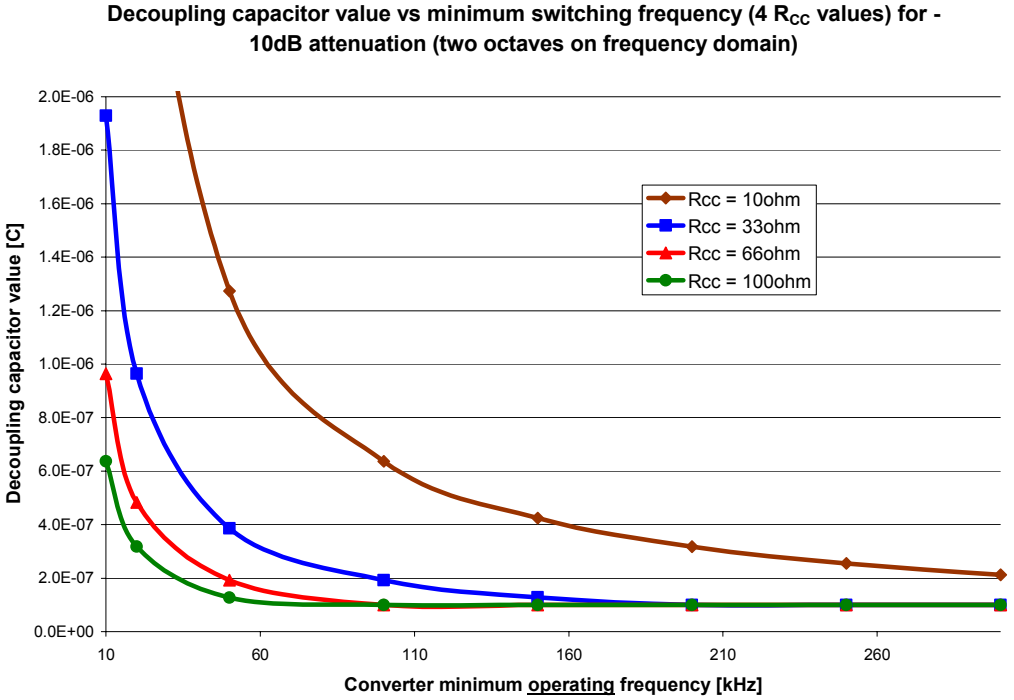


Figure 24: decoupling capacitor value vs. min. switching frequency, 10dB attenuation on supply.

In case of operations through aux winding or winding tap, decoupling capacitor should be sized in order to allow one switching period operation even in absence of main supply, within an acceptable voltage ripple ΔV_{CC}

$$C_{\min} = \frac{I_{CC}}{f_{SW_{\min}} \cdot \Delta V_{CC}}$$

e. MOT resistor

Being the MOT setting linear with the resistor value, the following relationship can be used

$$R_{MOT} = 2.5 \cdot 10^{10} t_{MOT}$$

f. Rectifier turn off maximum current slope calculation for CCM systems

In CCM systems, it is highly recommended to control secondary slope $\frac{dI_{SEC}}{dt}_{turnoff}$ when the SmartRectifier™ turns off, in order to maximize efficiency. Figure 25 shows turn off waveforms, where at given times:

- t_1: primary switch turns on
- t_2: secondary V_{DS} hits V_{TH1} threshold
- t_3: secondary V_{DS} and I_D reach zero

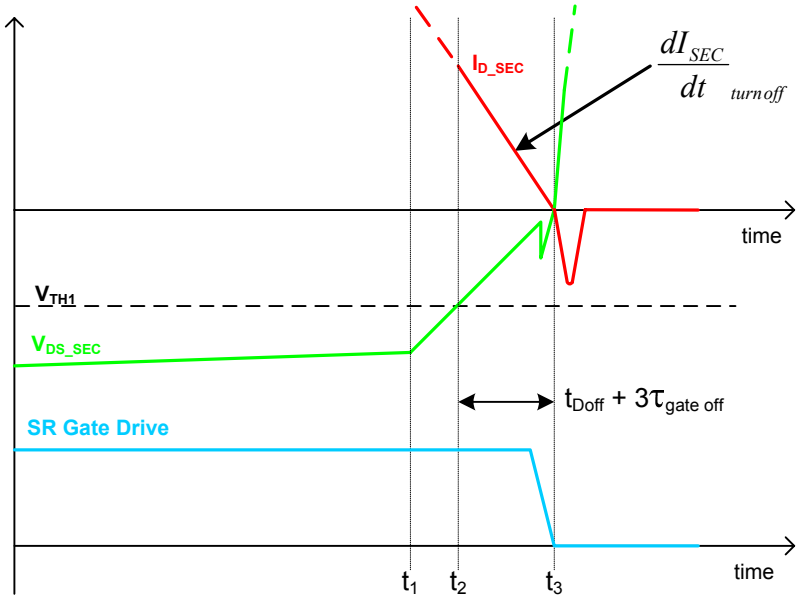


Figure 25: SmartRectifier™ turn off waveforms in dI/dt controlled CCM conditions.

It is evident, the optimal condition is to have synchronous FET turned off when the current approaches zero. In order to obtain this, $\frac{dV_{DS}}{dt}$ should be designed such as enough time is allowed to internal logic to react (t_{Doff} on IR1167 datasheet) and to gate driver to completely discharge the gate (3 times the gate loop time constant at turn off, i.e. $\tau_{gate\ off} = (R_{g\ FET} + R_g + r_{down}) \cdot C_{sync}$, where resistances are internal MOSFET gate resistance, external gate resistor and driver pull down resistance). This normally ends up to be in the range of 55 – 100ns.

The secondary current slope at turn of should therefore be designed according to

$$\left(\frac{dI_{SEC}}{dt}\right)_{turnoff} \leq \frac{V_{TH1}}{R_{DS\,on}(t_{Doff} + 3\tau_{gate\,off})}$$

In order to obtain this, a small saturable core in series with the primary winding could be used or a sufficiently rugged primary transistor with slow turn on for small power systems.

The primary maximum current slope requirement at turn on will be easily calculated using transformer turns ratio:

$$\left(\frac{dI_{PRI}}{dt}\right)_{turnon} = \frac{N_{SEC}}{N_{PRI}} \cdot \left(\frac{dI_{SEC}}{dt}\right)_{turnoff}$$

If this design condition is met, the reverse current through the Synchronous FET will be minimal and only needed for charging its output capacitance up to the reverse voltage.

Design example with IR1167AS (10.7V gate output voltage)

System data:

- $f_{SW_{\max}} = 250kHz$
- $MOT = 1.2\mu s$
- Critical Conduction Mode
- $f_{SW_{\min}} = 18kHz$
- $T_{IC_{amb}} = 80^{o}C$
- Low side rectifier system, output voltage 19V (direct supply from converter output possible)

Synchronous MOSFET: IRFB4110, 100V 4.5mΩ max

- $Q_g = 150nC$ @ $V_{gs} = 10V$
- $Q_{gd} = 43nC$ @ $V_{gs} = 10V$
- $C_{iss} = 9.62nF$; $R_{g_{FET}} = 1.3\Omega$

a. OVT setting: ground

b. IC current consumption calculation

$$C_{sync} = \frac{Q_g - Q_{gd}}{V_{gs}} = 10.7nF$$

$$I_{CC} = f_{SW_{\max}} C_{sync} V_{g_{high}} + \left(I_{QCC} + 7 \cdot 10^{-9} f_{SW_{\max}}\right) = 32.8mA$$

c. Gate and supply series resistors design and thermal verification

Assuming the total gate loop trace length is 15mm (0.6inch) therefore $L_g \approx 15nH$

$$R_{g_{loop}} > 2\sqrt{\frac{L_g}{C_{iss}}} = 2.5\Omega$$

From MOSFET datasheet internal gate resistance is 1.3Ω, from IR1167S datasheet driver pull down resistance is 0.7Ω, for a total of 2Ω. It looks therefore reasonable to chose an external gate resistor for the missing part

$$R_g = 0.5\Omega$$

According to the procedure, let's now verify the system thermally:

$$P_{dr} = 2 f_{SW\max} E_g = 306mW$$

Therefore

$$P_{R_g} + P_{R_{g\_FET}} = \left(\frac{R_g + R_{g_{FET}}}{R_g + R_{g_{FET}} + R_{Source}} + \frac{R_g + R_{g_{FET}}}{R_g + R_{g_{FET}} + R_{Sink}} \right) \cdot \frac{P_{dr}}{2} = 155mW$$

Assuming an acceptable IC maximum junction temperature of 130ºC

$$P_{IC_{\max}} = \frac{T_{J\max} - T_{IC\_amb}}{R_{\vartheta JA}} = 390mW$$

Which means a maximum V_{CC} voltage

$$V_{CC_{\max}} = \frac{P_{IC_{\max}} + (P_{R_g} + P_{R_{g\_FET}})}{I_{CC}} = 16.6V$$

This value is far away from the available 19V supply, and a series resistor would probably dissipate too much power. According to Figure 22, it is possible to slightly increase the gate resistor and get significant benefits. Let assume it is increased in value to

$$R_g = 1.1\Omega$$

The power dissipated in the gate loop resistance external to the IC will become

$$P_{R_g} + P_{R_{g\_FET}} = \left(\frac{R_g + R_{g_{FET}}}{R_g + R_{g_{FET}} + R_{Source}} + \frac{R_g + R_{g_{FET}}}{R_g + R_{g_{FET}} + R_{Sink}} \right) \cdot \frac{P_{dr}}{2} = 172mW$$

The maximum supply voltage will change to

$$V_{CC_{\max}} = \frac{P_{IC_{\max}} + (P_{R_g} + P_{R_{g\_FET}})}{I_{CC}} = 17.2V$$

It is reasonable now to “fill the gap” with 19V through a series resistor:

$$R_{CC} = 55\Omega$$

This resistor will dissipate a maximum of 60mW, which is considered acceptable.

d. Decoupling capacitor

Being the system powered from output, filtering criteria is the preferred one, therefore

$$C_{\min} = \frac{2}{\pi \cdot f_{SW_{\min}} \cdot R_{CC}} = 643nF$$

from which the next standardized value is chosen

$$C = 660nF$$

e. MOT resistor

From the given relationship

$$R_{MOT} = 2.5 \cdot 10^{10} t_{MOT} = 30k\Omega$$

Layout guidelines and examples

➢ *IC placement*

Due to the nature of the control, based on fast and accurate voltage sensing, it is mandatory to layout the circuit in order to keep the IR1167 as closest as possible to the SR MOSFET. As a general guideline, the physical distance between the two devices should never exceed 10mm (0.4 inches).

➢ *IC Decoupling Capacitor*

The key element to proper bypassing of the IC is the physical location of the bypass capacitor and its connections to the power terminals of the control IC. In order for the capacitor to provide adequate filtering, it must be located as close as physically possible to the V_{CC} and COM pins and connected thru the shortest available path.

➢ *Differential Sensing for V_D/V_S*

IR1167S provides accurate differential voltage sensing across synchronous MOSFET. It is recommended to minimize the traces lengths and to keep it separated from the power ground as much as possible. In case of through hole devices, the device pin would be the best place where V_S and GND traces connect.

If SO8 MOSFET is used, traces should be kept separated until the copper area where source pins are soldered.

For low side configurations, when a sensing resistor is used for current feedback in the rectifier power loop, it is highly recommended not to include it in the driving and sensing loops. This will cause some noise on the V_{CC}, which will be properly filtered by the decoupling capacitor and the R_{CC} series resistor, as shown in the Figure 26 schematic.

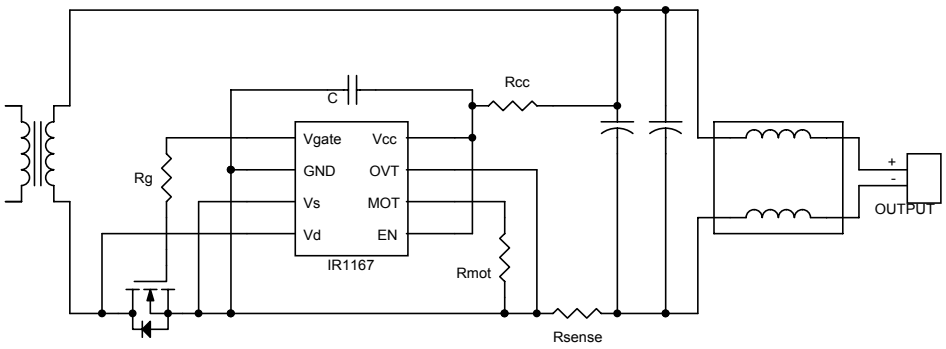


Figure 26: output current sense resistor placement (if present).

➢ *Gate Drive Loop*

Minimal gate drive loop will reduce requirements for damping, enhancing system robustness. Gate loop inductance plays a major role in damping requirements as shown in Figure 21. Once layout is finalized, then a "rule of thumb" estimation consists in measuring the physical loop trace length in assuming each millimeter (1mm = 39.37mils) accounts for 1nH. Other methods include measurement (low frequency RCL meters or current slope for a given voltage pulse) or FEM simulations.

➢ *Single layer board layout examples*

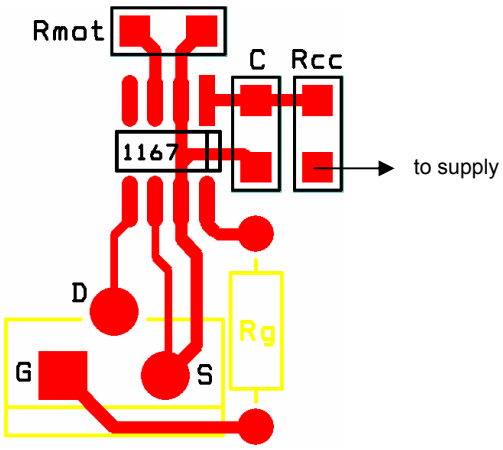


Figure 27: Single side board, TO220 MOSFET, OVT grounded, solder side view, through hole gate resistor.

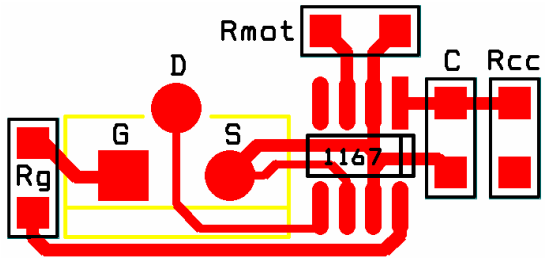


Figure 28: Single side board, TO220 MOSFET, OVT grounded, solder side view, SMD gate resistor.

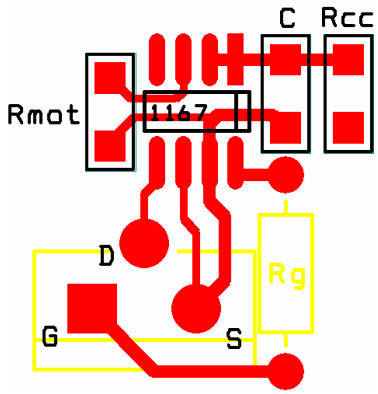


Figure 29: Single side board, TO220 MOSFET, OVT to VCC, solder side view, through hole gate resistor.

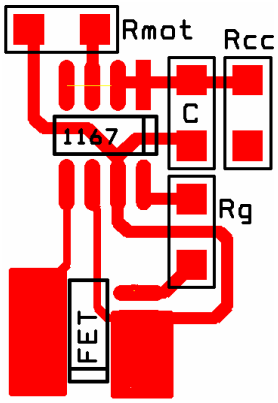


Figure 30: Single side board, SO8 MOSFET, OVT to VCC, solder side view.

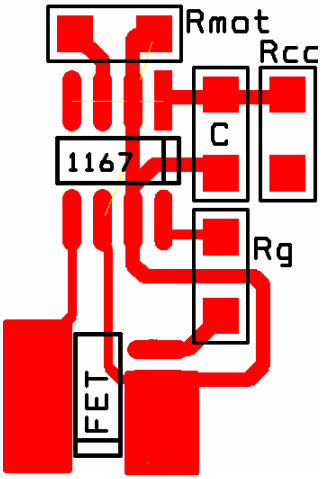


Figure 31: Single side board, SO8 MOSFET, OVT grounded, solder side view.

Symbols list

V_{TH1}: IR1167 turn off threshold
V_{TH2}: IR1167 turn on threshold
V_{TH3}: IR1167 periodic logic (reset) threshold
R_{DSon}: synchronous rectifier MOSFET channel ON resistance
I_D: synchronous rectifier MOSFET drain current
V_{DS}: synchronous rectifier MOSFET drain to source voltage
MOT: IR1167 minimum ON time parameter
t_{blank}: IR1167 turn off blanking time
T1: primary switch ON time in flyback converter
T2: secondary current duration in flyback converter
T3: primary AND secondary circuit inactivity time in DCM flyback converter
C: IR1167 decoupling capacitance value on supply
R_g: SR MOSFET gate drive loop resistance external to IR1167 IC
R_{MOT}: Minimum ON Time programming resistor value
R_{CC}: supply voltage series resistor value (V_{supply} to V_{CC})
f_{SWmax}: converter maximum operating switching frequency
f_{SWmin}: converter minimum operating switching frequency
T_{ICamb}: ambient temperature with reference to IC (most cases is PCB temperature where IC is soldered)
V_{supply}: available voltage source for IC power up
OVT: Offset Voltage Trimming of turn on and off comparator
Q_g: SR MOSFET total gate charge
Q_{gd}: SR MOSFET gate to drain (Miller) charge

V_{gs}: SR MOSFET gate to source voltage
V_{g_high}: IR1167 gate drive output voltage
I_{QCC}: IR1167 quiescent current
$R_{g\ loop}$: total gate loop resistance
L_g: total gate loop parasitic inductance
C_{iss}: SR MOSFET input capacitance
E_g: SR MOSFET stored in gate
P_{dr}: total power dissipated by the gate drive function
R_{Source}: gate driver source resistance
R_{Sink}: gate driver sink resistance
P_{Rg}: gate resistance dissipated power
P_{ICmax}: IR1167 IC maximum power dissipation
T_{IC_amb}: IC environment temperature (PCB temperature)
$R_{\theta JA}$: IR1167 IC junction to ambient thermal resistance
V_{CC}: supply voltage on IR1167 pin
I_{CC}: supply current on IR1167 pin
UVLO: IR1167 Under Voltage Lock Out
V_{supply}: system available supply voltage for SR function
C_{min}: minimum calculated decoupling capacitance
ΔV_{CC}: supply peak to peak ripple voltage on IR1167 V_{CC} pin
t_{MOT}: obtained minimum on time
$\tau_{gate\ off}$: gate loop turn off time constant
N_{SEC}: transformer secondary winding number of turns
N_{PRI}: transformer primary winding number of turns

References

[1] IR1167S Smart Rectifier control IC datasheet, International Rectifier, February 2006

[2] M.T. Zhang, M. Jovanovic, F. Lee, “Design considerations and performance evaluations of Synchronous Rectification in Flyback converters”, IEEE Transactions on Power Electronic, VOL.13, N.3, May 1998

[3] Smart Rectifier™ increases Power Density in Flyback Topologies while reducing System Complexity, Maurizio Salato, Adnaan Lokhandwala, Marco Soldano, and Helen Ding, PCIM China 2006

[4] Novel Output Rectification Control IC Improves Efficiency & Thermal Performance in External AC-DC Power Supplies, Adnaan Lokhandwala, Maurizio Salato and Marco Soldano, Portable Power Developers Conference 2006

[5] US Patent Application Publication N. 2005/0122753 A1, Jun. 9, 2005

Rev. 1.1 – March 2006