USB 3.0

SuperSpeed USB 3.0 Specification Revolutionizes An Established Standard

Sanjiv Kumar
Nov. 2008

denali

Overview

The Universal Serial Bus (USB) 3.0 specification is a new industry-standard peripheral connection technology, developed by USB Implementers Forum, for connecting peripherals to PCs and laptops. The USB 3.0 specification draws from the same architecture of the wired USB specification and therefore is a backward-compatible standard with the same ease-of-use and plug and play capabilities of previous USB technologies, but with a 10X performance increase and lower power consumption. The USB 3.0 specification uses two additional high-speed differential pairs for SuperSpeed mode, which boosts its bandwidth to 5 GB/s.

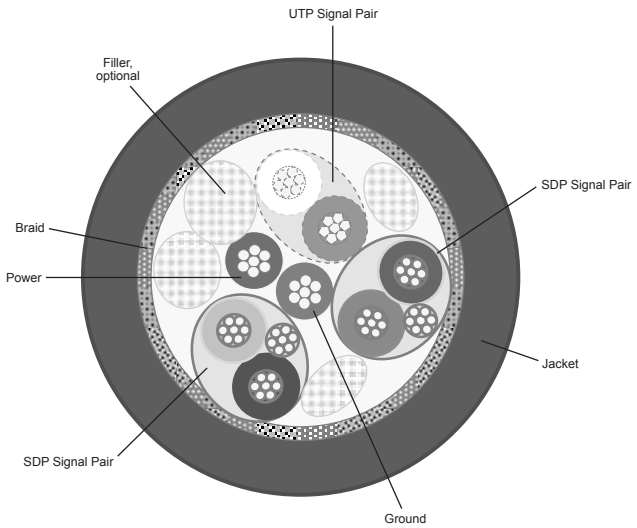
For end-users of the USB 3.0 specification, the goals of connecting peripherals with PCs or laptops are still the same as the Hi-Speed (USB 2.0) specification, but with significantly increased speed and reduced power consumption. The SuperSpeed USB specification, therefore, is not simply an upgrade to earlier versions of the USB 2.0 specification. Due to the broad deployment of USB 2.0 devices in the market, SuperSpeed USB devices need to be backward compatible, but the backward compatibility portion of the SuperSpeed USB specification targets only the device drivers and connector architecture. The higher speed and reduced power consumption for the USB 3.0 specification uses advanced mechanisms and techniques similar to ones that were used for other high bandwidth interfaces, such as the PCI Express (PCIe) specification. As a result, the SuperSpeed USB specification has many differences compared to earlier generations of USB specifications (1.1/2.0/OTG).

The scope of this paper is to clearly explain some of the key differences between the new USB 3.0 specification and earlier USB generations. Additionally, this article identifies the main similarities between USB 3.0 and PCI Express (PCIe).

Differences between SuperSpeed USB and USB 2.0

As mentioned earlier, the SuperSpeed USB specification is similar to earlier USB versions in terms of the connector and device drivers. The end-user and device driver engineer may find SuperSpeed USB similar to earlier versions, but it is significantly different to implementers of SuperSpeed USB host and devices.

At a mechanical level, the SuperSpeed USB specification supports a dual-bus architecture for backward compatibility to a USB 2.0 device. This means that the SuperSpeed USB cable needs to support eight primary wires, two wires for USB 2.0 connectors, two shared between the USB 2.0 and SuperSpeed USB specifications (PWR and GND) and four for SuperSpeed USB dual-simplex differential signals. The SuperSpeed USB specification supports a dual-simplex data-interface with four differential wires for simultaneous data flow in both directions. It should be noted that adding a bi-directional data interface was necessary to support the SuperSpeed USB specification's target speed because the half-duplex, two wire differential signals of USB 2.0 and unidirectional data flow were not enough to support the SuperSpeed USB specification's high bandwidth.



Many changes were required in the existing USB 2.0 data flow to maximize the advantages of the SuperSpeed USB bi-directional dual-simplex data interface. Though the SuperSpeed USB specification is still a host directed protocol and preserves the concepts of endpoints, pipes transfer types, etc., the traffic flow has changed to asynchronous as opposed to polling traffic flow in previous USB specifications. In addition, there are many fundamental differences at the Protocol level as shown in the following table:

SuperSpeed	USB 2.0
Dual-simplex, unicast protocol	Full-duplex, broadcast protocol
Uses asynchronous notification (NRDY, ERDY)	Uses polling mechanism
Supports streaming for bulk transfers	Does not support streaming
Supports continuous bursting	Does not support bursting
For OUT, token is integrated into data	OUT is three seperate parts (Token, Data, and Handshake)
For IN, token is replaced by Handshake	IN is three seperate parts (Token, Data, Handshake)
Splits error detection, recovery and flow control functionality between protocol layer and link layer	Protocol layer manages error detection, recovery, and flow control functionality

SuperSpeed also manages power consumption more efficiently, which results in some differences at the Protocol level.

1. SuperSpeed supports link level power management, which means either a host or a device can initiate link power management. In USB 2.0, it is always initiated by the host.

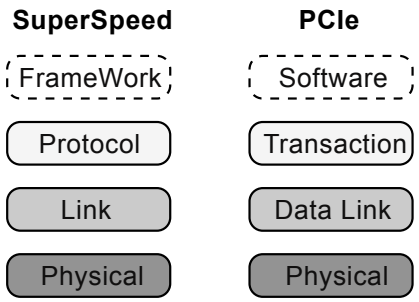
2. SuperSpeed USB allows isochronous devices to enter in the low power link states between service intervals. This mechanism is not supported in USB 2.0.

3. SuperSpeed USB allows devices to inform the host of their latency tolerance using the Latency Tolerance Messaging mechanism. This allows the host to enter in low power states for better power performance.

Similarities between SuperSpeed and PCI Express

Because of the inherent bandwidth limitations in the USB 2.0 specification, developers of the USB 3.0 specification decided to pattern the new USB 3.0 protocol on the PCIe architectural structure to attain the higher 5Gb/s bandwidth and lower power demands of the SuperSpeed USB specification. Both the SuperSpeed USB and the PCIe specifications, therefore, are derived from the basic OSI layered architecture. Both protocols look very similar in terms of layer architecture, and their physical layers share many common functions, as well as similar concepts for other layers. Due to the different intent of the two specifications, the functional details of their link and protocol layers vary but the goals of each specification are the same, namely increased bandwidth and lower power consumption.

High Level View of Architectures (SuperSpeed vs. PCI Express specifications)



The Protocol layer of the SuperSpeed USB specification and the Transaction layer of the PCIe specification are the uppermost layers of the two architectures. They each begin the process of turning request or data packets from software or device drivers into protocol specific transactions. The communications of these layers (Protocol for the SuperSpeed USB specification and Transac-

tion for the PCIe specification) are accomplished via an exchange of packets. Obviously, due to protocol differences, the packet types and formats differ between the Protocol layer of the SuperSpeed USB specification and the Transaction layer of the PCIe specification.

The Link layer of both protocols is responsible for data integrity, flow control, error correction and detection. Some of the SuperSpeed USB features listed below are similar to the PCIe specification, and are covered in the Link layer of the SuperSpeed specification. The PCIe specification addresses these features in the Physical layer. For example:

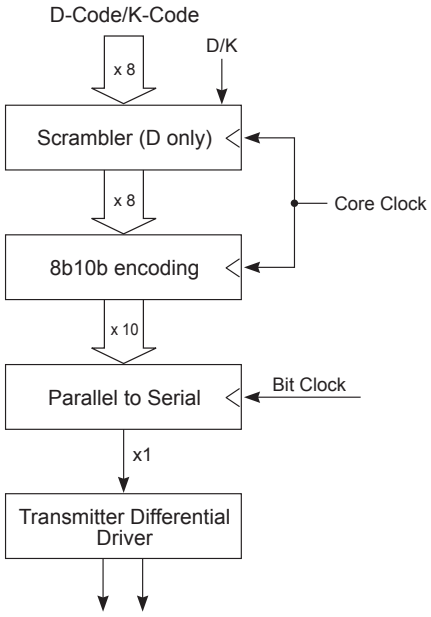
- Link initialization
- Packet framing
- LTSSM specification
- Link error rules/recovery

Both protocols define the Link Training and Status State Machine (LTSSM) that contains various similar states for link initialization, recovery, loopback, hot reset, compliance, disable, and power management. The training sequences consist of ordered sets defined in each protocol. Also, both protocols use special symbols (K-codes) for framing, link management, and similar mechanisms to achieve Bit/Symbol lock, lane polarity inversion, and clock recovery from the incoming data stream.

Both the SuperSpeed USB and the PCIe specifications support power management at the link and device levels. There are subtle differences due to protocols, but most of the concepts remain similar in terms of power management's link states and entry/exit of power states.

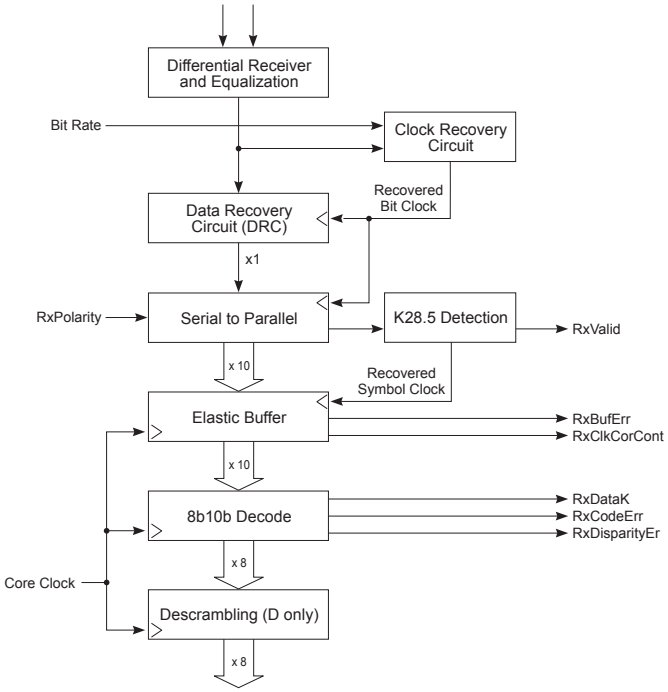
The transmitter and receiver blocks of both protocols are exactly the same and most of their components have a lot in common. The following figures illustrate the transmitter and receiver blocks.

Transmit Block



Superspeed and PCIe Transmitter Block

Receiver Block



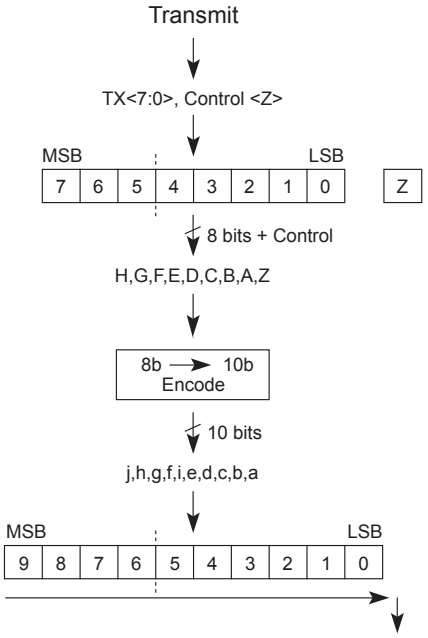
SuperSpeed and PCIe Receiver Block

As briefly mentioned above, the receiver and transmitter of both the SuperSpeed USB and the PCIe specifications have the following features which are exactly the same across both protocols.

- 8b/10b symbol encoding/decoding
- Serialization and de-serialization of data
- Data scrambling

8b/10b Symbol Encoding/Decoding

The main purpose of 8b/10b encoding is to embed a clock signal into a data stream. Encoding the clock signal into data streams renders external clocks unnecessary. Since both protocols embed the clock in the data stream, both of these use 8b/10b transmission code, identical to that specified in ANSI X3.230-1994, clause 11. Thus, the 8b/10n encoding mechanism is exactly the same for the SuperSpeed USB and PCIe specifications.

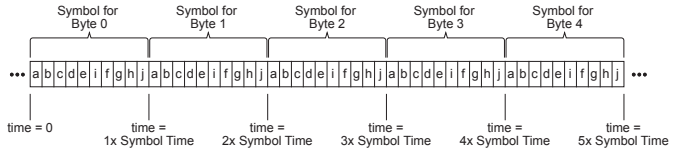


SuperSpeed and PCIe 8b/10b Encoding

Serialization and De-serialization of Data

The SuperSpeed USB and PCIe specifications implement serialization and de-serialization schemes in both protocols and act the same way.

The bits of a symbol are placed starting with bit "a" and ending with bit "j".

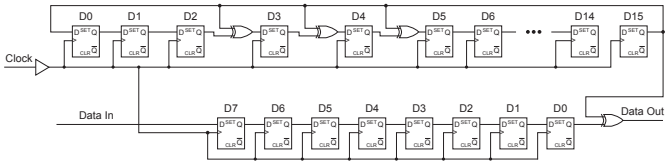


SuperSpeed and PCIe bit Serialization

Data Scrambling

Both the SuperSpeed USB and PCIe specifications use the same data scrambling technique to reduce the possibility of electrical resonance on the link. Both protocols define scrambling/descrambling using a free running Linear Feedback Shift Register (LFSR). The LFSR implements the following polynomial:

$$G(X)=X^{16}+X^5+X^4+X^3+1$$



SuperSpeed and PCIe Data Scrambling (LFSR)

The PCI Express specification uses its PIPE interface to separate PHY from the other layers. The SuperSpeed USB specification also plans to use an interface which is very similar to PIPE.

Summary

For end-users and system software engineers, the SuperSpeed USB specification may look similar to its earlier generation. However, for the device/host implementers, it will be significantly different compared to earlier versions of the USB specification. See image below highlighting the similarities between SuperSpeed USB to USB 2.0 and PCIe (see figure below).

In order to dramatically boost performance and reduce power consumption, the USB 3.0 specification draws heavily from the functional superiorities of the PCIe specification. As a result, people who use USB 3.0 peripherals will see that it is not merely an evolution of previous versions of the USB protocol, but a vastly superior reinvention of the standard, with all of the performance advantages that today's high-speed systems require.

Author

Sanjiv Kumar, a 12 year veteran of the EDA industry joined Denali Software in January 2004 and currently serves as director of verification IP products.