AN-7015

Understanding the Complex Phenomenon of Shoot Through Full Equivalent Circuit Analysis

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Introduction

Equations today do not take into the account the effect of parasitic inductance on the gate and source circuits. This application note explores an approach that allows for the derivation of simple practical equations to calculate the gate voltage during the high side MOSFET turn on and hence, the propensity of the synchronous rectifier MOSFET for shoot through. This application note puts forth several solutions that take into account such inductances and allows a better understanding of this complex phenomenon. This application note will demonstrate that the gate inductance tends to make the situation worse while the source inductance helps keep the gate-source voltage at a lower level. This application note proposes an equation that describes the gate voltage in time as a function of all the circuit parameters.

The simplified schematics in Figure 1 and Figure 1b are used to derive the transient gate voltage equations in a progressively complex fashion. Figure 1 has both the gate inductance Lg and the source inductance Ls. By solving the two sets of equations that describe these two situations and comparing them, a better understanding of the shoot through phenomena and the individual effects of each of the parasitic inductances can be achieved.

What this Application Note will do:

- Examine Parasitic Inductance and the Phenomenon of Shoot Through
- Explore the Role of Gate Inductance and Source Inductance
- Demonstrate mathematically how gate voltage in time is a function of all circuit parameters

Figure 1b shows a very simplified circuit in the first attempt to calculate shoot through. In this example, source inductance is ignored. This is commenced by writing a set of differential equations e1..e3 as follows:

$$e1 := Id(t) + Co\left(\frac{d}{dt}Vd(t)\right) + Cgd\left(\left(\frac{d}{dt}Vd(t)\right) - \left(\frac{d}{dt}Vg(t)\right)\right) = 0$$

$$e2 := \frac{Vg(t) - Va(t)}{Rg} + Cgs\left(\frac{d}{dt}Vg(t)\right) + Cgd\left(\left(\frac{d}{dt}Vg(t)\right) - \left(\frac{d}{dt}Vd(t)\right)\right) = 0$$

$$e3 := \frac{Va(t)}{Lg} + \frac{\left(\frac{d}{dt}Va(t)\right) - \left(\frac{d}{dt}Vg(t)\right)}{Rg} = 0$$

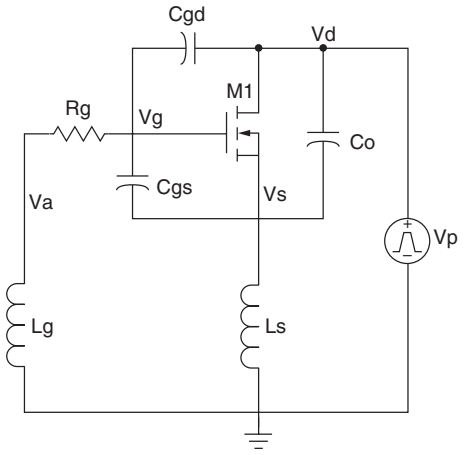


Figure 1. Schematic used in equation derivation with Source and Gate inductance

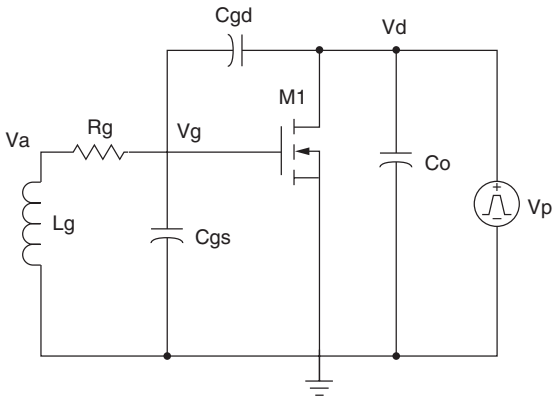
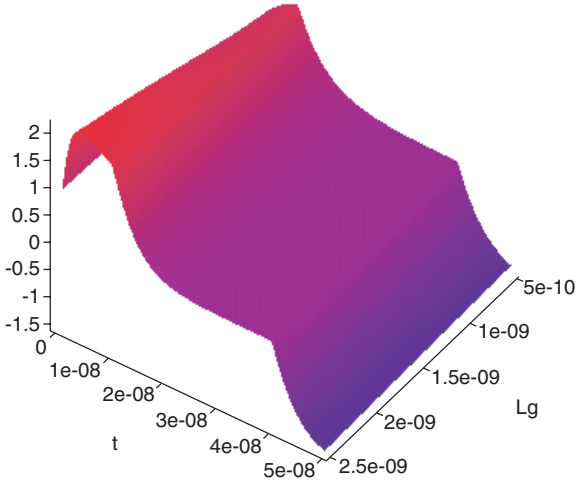


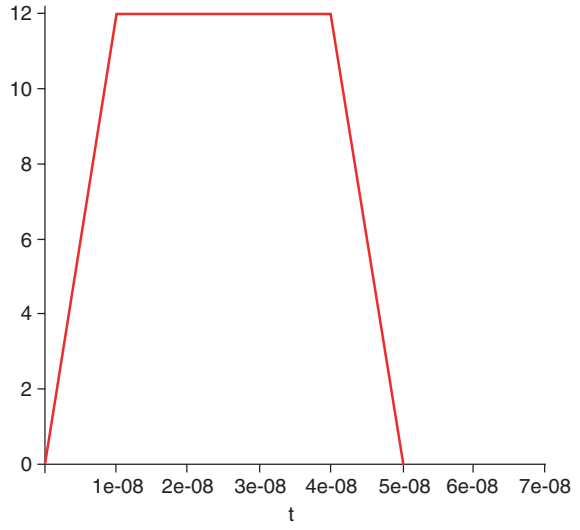
Figure 1b. Schematic used in equation derivation with Gate inductance only

Only the linear model of all capacitors was used to facilitate the exact solution.

By solving these three differential equations twice and assuming that Vp, the driving voltage, in the first case to be a single pulse of 12Volt and rise time of 10nS (Figure 2), and in the second case the rise time is1nS (Figure 3). Figure 2 shows a shoot through gate voltage of about 2 volts while Figure 3 shows a gate shoot through voltage of about 14 Volts, which is clearly due to the resonance of the gate inductance Lg with the inter-electrode capacitors. Both of these cases are not realistic and are not encountered in real life circuits. The explanation is very clearly the exclusion of the source inductance Ls.

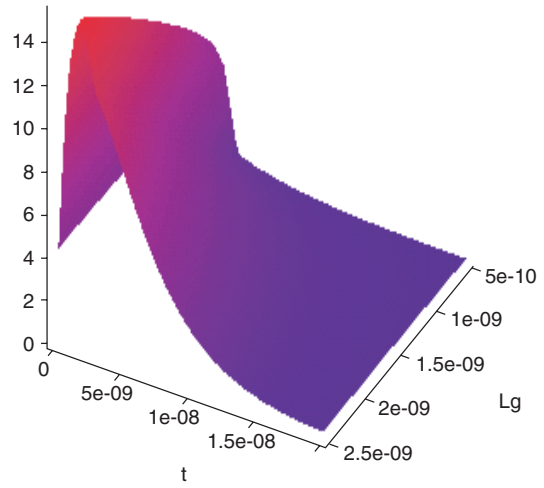


(a)

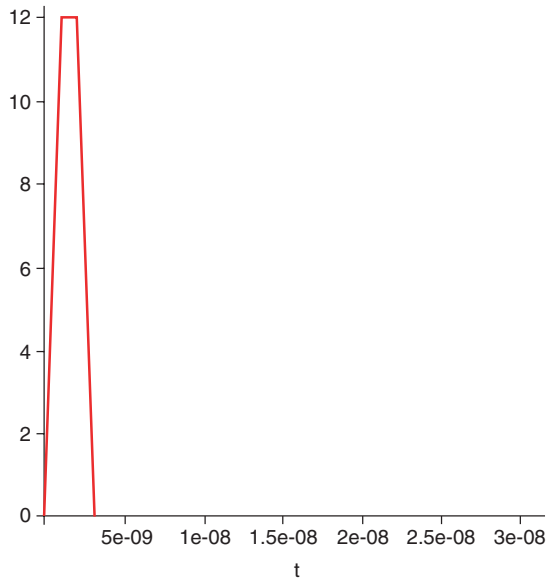


(b)

Figure 2. Gate voltage (a) and the Drain Driving Waveform (b)



(a)



(b)

Figure 3. where Ls = 2.5nH

In order to verify the assumption of the necessity of the source inductance in the circuit as in Figure 1 was included. In order for us to fully understand the mechanics of shoot through under these conditions, several conditions of input voltage was solved. In the first case below, only the rising edge of Vp was considered and the equations were solved accordingly.

And now the equations for Figure 1 as follows:

$$Vd(t) := \frac{Vm\,t}{tr}$$

$$e1 := Id(t) + Co\left(\frac{Vm}{tr} - \left(\frac{d}{dt}Vs(t)\right)\right) + Cgd\left(\frac{Vm}{tr} - \left(\frac{d}{dt}Vg(t)\right)\right) = 0$$

$$e2 := Co\left(\frac{d^2}{dt^2}Vs(t)\right) + Cgs\left(\left(\frac{d^2}{dt^2}Vs(t)\right) - \left(\frac{d^2}{dt^2}Vg(t)\right)\right) + \frac{Vs(t)}{Ls} = 0$$

$$e3 := \frac{Vg(t) - Va(t)}{Rg} + Cgs\left(\left(\frac{d}{dt}Vg(t)\right) - \left(\frac{d}{dt}Vs(t)\right)\right) + Cgd\left(\left(\frac{d}{dt}Vg(t)\right) - \frac{Vm}{tr}\right) = 0$$

$$e4 := \frac{Va(t)}{Lg} + \frac{\left(\frac{d}{dt}Va(t)\right) - \left(\frac{d}{dt}Vg(t)\right)}{Rg} = 0$$

Where:

Vm = Maximum Gate Drive voltage
Cgs = Gate to Source capacitance
Co = Drain to Source capacitance
Lg = Total Gate inductance
tr = Driving voltage rise time
Cgd = Gate to Drain capacitance
Rg = Total Gate series resistance
Ls = Total Source inductance

The gate drive voltage is a linear ramp with respect to time t.

By solving equations e1…e4 we get all the node voltages as a function of time t and the rest of the circuit parameters. Unfortunately the resulting equations are too long and complex to fully visualize.

In order for us to understand the effects of both the source inductance Ls and the gate inductance Lg, a couple of graphs can be generated to show the trends.

Figure 5 (a) shows the shoot through gate voltage for a rise and fall time of 10nS and a total drain voltage transient of 19 Volt. This level is quite realistic and agrees with lab results very well. Figure 5 (b) is the current in the driving voltage Vp. This is the current that usually flows in the high side MOSFET while turning on adding one further component to the dynamic losses.

The situation is much more complicated when we drive the low side MOSFET with a 19V at a rise time of 1nS. As can be seen from Figure 1, the current that flows in Co also flows in Ls adding one more complexity to the solution since this current tends to be beneficial from the shoot through point of view since it tends to raise the source voltage and hence mitigating the situation by allowing higher gate voltage without encountering shoot through. As a matter of fact under the right conditions of Ls and Lg, a negative Gate-Source voltage could be arrived at, which completely blocks any chance of the MOSFET turning on as can be seen in Figure 4.

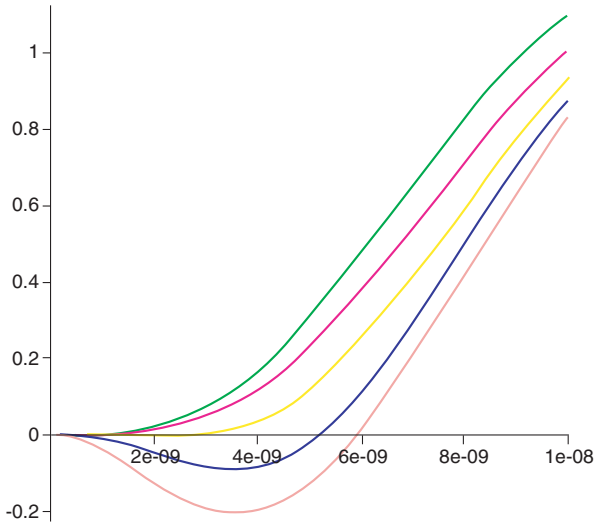
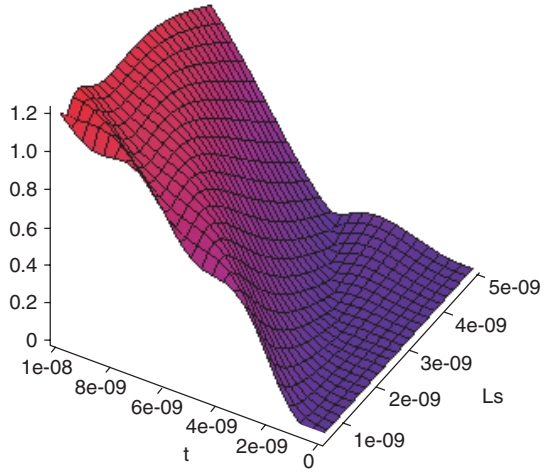


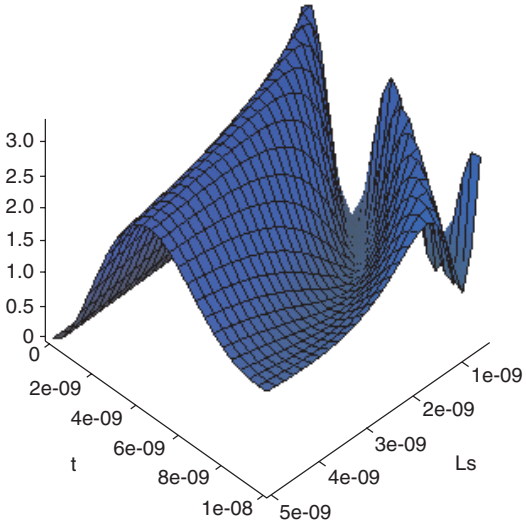
Figure 4. Gate-Source voltage at different combinations of Lg and Ls. Notice the blue and red plots going negative for part of the cycle

Figure (a) represents the gate-source voltage when the rise and fall time is 1nS. This transition time is very close to the current high performance circuit conditions where 3nS–5nS is encountered on a regular basis. Within the next few years, a sub nanosecond transitions will be the norm in high performance DC/DC power supplies. Notice that the shoot through gate-source voltage is much smaller than in the 10nS rise time case because of the effect of Co on the current flowing in the source inductance Ls. On the other hand

Figure 6 (b) represents the current in the driving voltage Vp that, as mentioned before, flows normally in the high side MOSFET. Notice that this current, under very low source inductance conditions may go as high as 16Amp adding significant amount of losses to the high side MOSFET turn on losses. This is clearly an undesirable side effect since as can be seen in [2] a very low source inductance is desirable for fast turn on/off. As it is always the case with any engineering problem, a compromise between all of these effects must be reached and in order to do this, one needs to fully understand all the underlying issues and problems and use this knowledge to our advantage.

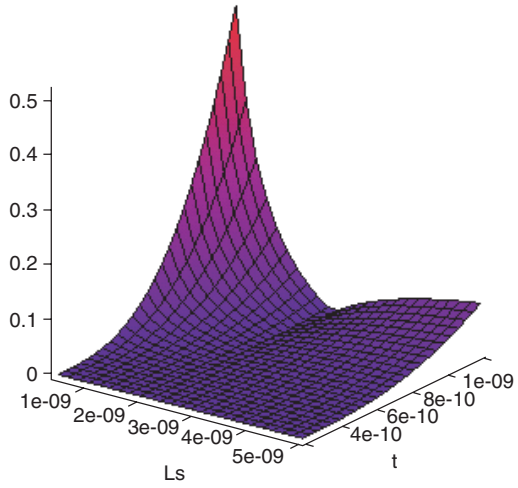


(a)

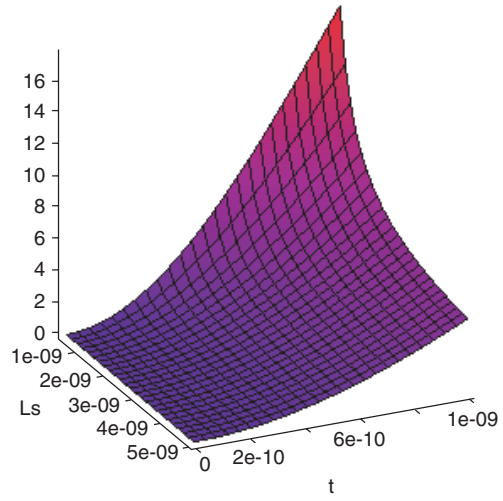


(b)

Figure 5. Gate voltage and current in the driving source Vp. tr=10nS



(a)



(b)

Fig. 6 Gate voltage and current in the driving source Vp. tr=1nS

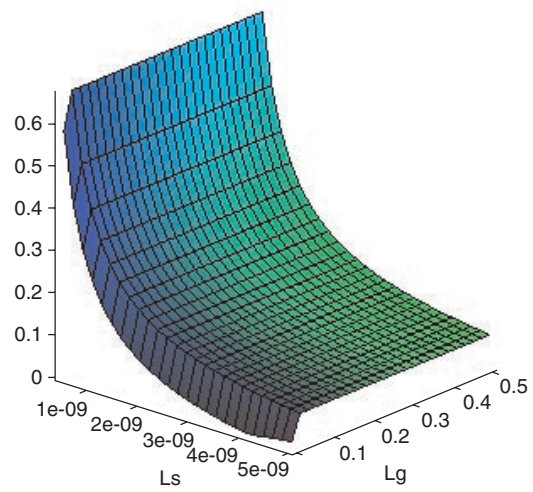


Fig. 7 Gate voltage as a function of gate inductance Lg and source inductance Ls. tr=1nS

Now that one has a understanding of the shoot through phenomenon with the inclusion of both Lg and Ls, one needs to understand the relative influence of each of these parasitic inductances. Figure 7 shows the shoot through gate-source voltage as a function of Lg and Ls at the end of the rise time of 1nS. It can be clearly seen that except for very low Lg < 1nH, the gate-source voltage is dominated by the source inductance Ls where the larger Ls is the smaller the gate-source voltage and the less possibility of the shoot through occurring.

Figure 8 shows the gate-ground voltage in the case of 10nS rise time. When compared to Figure 5 (a) showing the gate - source voltage under identical conditions, it becomes evident that measuring the gate-ground voltage of 2.5 Volt and predicting the existence of shoot through based on the fact that the gate-ground Voltage is larger than the gate threshold voltage (Vgth) is incorrect since Figure 5 (a) clearly indicates that the gate-source voltage is about 1.2 Volts only and hence, for a MOSFET with minimum Vgth of say 1.5 Volt there will be no shoot through though the Gate-Ground voltage is 2.5 Volt

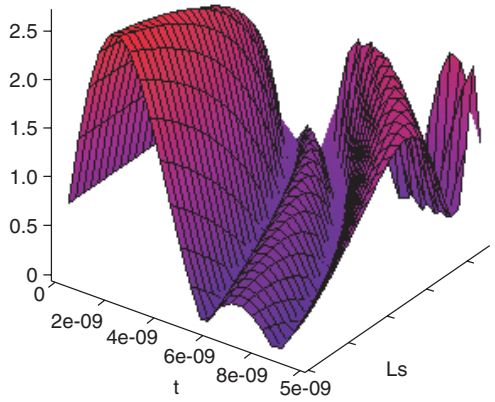


Figure 8. Gate to Ground voltage for Wide pulse. tr=10nS

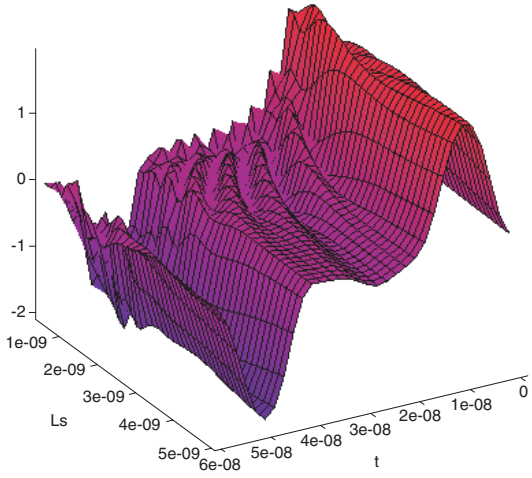


Figure 9. Gate to Source voltage for Wide pulse. tr=10nS

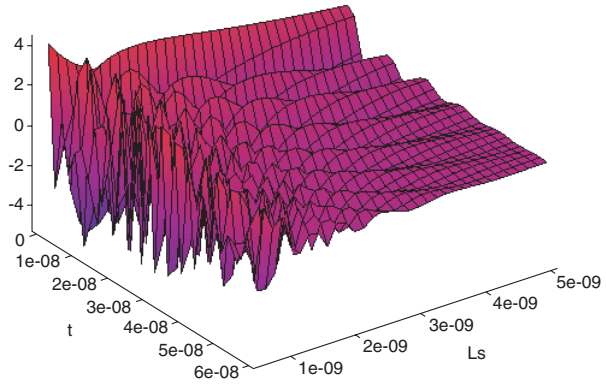


Figure 10. Gate to source voltage for a very narrow pulse. tr=1nS

For completion Figures 9 and 10 are included. Figure 9 shows the gate-source voltage when the driving voltage is a single pulse with rise and fall time of 10nS while in Figure 10 the rise time is 1nS using the circuit in Figure 1 with both Lg and Ls present. Both graphs show that shoot through is likely to take place when Ls is very small i.e. < 1nS. Figure 10 shows the complexity of gate-source voltage waveform as Ls varies from 0.5nH to 5nH.

This application note attempts to explain just shoot through in the presence of Lg and Ls without any attempt to explain other aspects of this phenomenon that can easily be gleaned from the above graphs

Conclusions

The gate-ground voltage alone does not tell whether shoot through will take place or not but rather the gate-source voltage is the decisive factor. Although this conclusion is very obvious, it is not observed in the lab since the source of the synchronous rectifier is always connected to ground, gate-ground voltage is usually measured. Source inductance plays a more pronounced role in determining whether shoot through occurs or not due mainly to the effect of Co and Ls.

A source inductance larger than zero is desirable even though this will cause larger switching losses since shoot through generates prohibitively larger losses than switching losses.

A thorough and complete understanding of the parasitic inductances of all our packages is mandatory to evaluate the susceptibility of a given MOSFET in a given package to shoot through in preparation for the sub 1nS switching of the future. Combining the shoot through loss mechanism with reverse recovery loss mechanism, it becomes obvious that some loop inductance is mandatory to mitigate the switching losses. Exactly how much inductance is needed depends on the circuit and the individual MOSFETs and Gate Drivers utilized in the application. There is a large current component that the high side MOSFET has to deliver to charge all the inter-electrode capacitors. This current is

dependant on the rise time of the voltage of the junction between the high side and the low side MOSFETs and may become the dominant switched current in the high side MOSFET for rise times of <1nS

References

[1] Evaluating MOSFET Susceptibility for Cross-Conduction, *Alan Elbanhawy, Fairchild Semiconductor International, PCIM Magazine, Europe*

[2] Loss Mechanism of the Synchronous Buck Converter Under the Microscope, *Alan Elbanhawy, Fairchild Semiconductor International*

Appendix A: The following equations describe the Gate-Ground Voltage (Vgs), The Source-Ground voltage (Vss), Gate-Source voltage (Vgss) and the current through the driving voltage (Ids) in the s or Laplace domain. The inverse Laplace solution from which the graphs above were calculated is far too complex to be shown here.

$$Vgs := \frac{(Rg + s\,Lg)\,(Cgd + Co\,Ls\,s^2\,Cgd + Cgs\,s^2\,Ls\,Cgd + Cgs\,s^2\,Ls\,Co)\,Vm}{s\,tr\,(Lg\,s^4\,Cgd\,Cgs\,Ls + Lg\,s^4\,Cgd\,Co\,Ls + Cgs\,s^2\,Lg + Lg\,Cgs\,s^4\,Co\,Ls + s^3\,Cgs\,Rg\,Co\,Ls + s\,Cgs\,Rg + s^3\,Cgd\,Rg\,Co\,Ls + s^3\,Cgd\,Rg\,Cgs\,Ls + s\,Cgd\,Rg + s^2\,Cgd\,Lg + Co\,Ls\,s^2 + Cgs\,s^2\,Ls + 1)}$$

$$Vss := \frac{Ls\,Vm\,(Lg\,Cgs\,s^2\,Cgd + Cgs\,s\,Rg\,Cgd + Co + Lg\,s^2\,Cgd\,Co + Lg\,Cgs\,s^2\,Co + s\,Cgs\,Rg\,Co + s\,Cgd\,Rg\,Co)}{tr\,(Lg\,s^4\,Cgd\,Cgs\,Ls + Lg\,s^4\,Cgd\,Co\,Ls + Cgs\,s^2\,Lg + Lg\,Cgs\,s^4\,Co\,Ls + s^3\,Cgs\,Rg\,Co\,Ls + s\,Cgs\,Rg + s^3\,Cgd\,Rg\,Co\,Ls + s^3\,Cgd\,Rg\,Cgs\,Ls + s\,Cgd\,Rg + s^2\,Cgd\,Lg + Co\,Ls\,s^2 + Cgs\,s^2\,Ls + 1)}$$

$$Vgss := \frac{(Rg + s\,Lg)\,(Cgd + Co\,Ls\,s^2\,Cgd + Cgs\,s^2\,Ls\,Cgd + Cgs\,s^2\,Ls\,Co)\,Vm}{s\,tr\,(Lg\,s^4\,Cgd\,Cgs\,Ls + Lg\,s^4\,Cgd\,Co\,Ls + Cgs\,s^2\,Lg + Lg\,Cgs\,s^4\,Co\,Ls + s^3\,Cgs\,Rg\,Co\,Ls + s\,Cgs\,Rg + s^3\,Cgd\,Rg\,Co\,Ls + s^3\,Cgd\,Rg\,Cgs\,Ls + s\,Cgd\,Rg + s^2\,Cgd\,Lg + Co\,Ls\,s^2 + Cgs\,s^2\,Ls + 1)}$$

$$Ids := \frac{Ls\,Vm\,(Lg\,Cgs\,s^2\,Cgd + Cgs\,s\,Rg\,Cgd + Co + Lg\,s^2\,Cgd\,Co + Lg\,Cgs\,s^2\,Co + s\,Cgs\,Rg\,Co + s\,Cgd\,Rg\,Co)}{tr\,(Lg\,s^4\,Cgd\,Cgs\,Ls + Lg\,s^4\,Cgd\,Co\,Ls + Cgs\,s^2\,Lg + Lg\,Cgs\,s^4\,Co\,Ls + s^3\,Cgs\,Rg\,Co\,Ls + s\,Cgs\,Rg + s^3\,Cgd\,Rg\,Co\,Ls + s^3\,Cgd\,Rg\,Cgs\,Ls + s\,Cgd\,Rg + s^2\,Cgd\,Lg + Co\,Ls\,s^2 + Cgs\,s^2\,Ls + 1)}$$

$$\frac{Vm\,(Co\,Ls\,s^2\,Cgd + Cgs\,s^2\,Ls\,Cgd + Cgd + Co + Lg\,Cgs\,s^2\,Cgd + Cgs\,s\,Rg\,Cgd + Lg\,s^2\,Cgd\,Co + Lg\,Cgs\,s^2\,Co + s\,Cgs\,Rg\,Co + s\,Cgd\,Rg\,Co + Cgs\,s^2\,Ls\,Co)}{tr\,s\,(Lg\,s^4\,Cgd\,Cgs\,Ls + Lg\,s^4\,Cgd\,Co\,Ls + Cgs\,s^2\,Lg + Lg\,Cgs\,s^4\,Co\,Ls + s^3\,Cgs\,Rg\,Co\,Ls + s\,Cgs\,Rg + s^3\,Cgd\,Rg\,Co\,Ls + s^3\,Cgd\,Rg\,Cgs\,Ls + s\,Cgd\,Rg + s^2\,Cgd\,Lg + Co\,Ls\,s^2 + Cgs\,s^2\,Ls + 1)}$$