Remote FPGA Reconfiguration Using MicroBlaze or PowerPC

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Summary

Field upgradeability is one of the key features of recent FPGA based systems. This application note describes techniques for remote FPGA reconfiguration through an Ethernet port. Remote reconfiguration as demonstrated in this document will require the use of either MicroBlaze™ or PowerPC™ embedded processors, external Flash, SDRAM memory, and a Xilinx CPLD. "Watch-dog" monitoring is included in the solution.

This application note also presents a system level solution using a Xilinx CPLD and Flash memory to configure and monitor Xilinx FPGA configuration status.

Introduction

For this application note, we made a special daughter card, which can be plugged into a P-160 module connector on an Insight Virtex™-II Pro development board. But, you can design and build your own system using this application note. The main target of our reference design is Wireless BTS, but you can target any other system which requires a remote FPGA reconfiguration solution.

<table>
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<th>Table 1: Supported Devices</th>
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<td><strong>MicroBlaze Processor</strong></td>
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<td><strong>PowerPC Processor</strong></td>
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RFCS (Remote FPGA Configuration System) System Overview

There are five main devices in this system:

- **Target FPGA**: The target FPGA is used to implement the main user design. It also incorporates the MicroBlaze or PowerPC processor with GPIO, EMC, UART, EMAC and the SDRAM controller
- **CPLD**: The CPLD is used to implement the FPGA reconfiguration, and perform hardware and software configuration watch-dog and status monitoring. This design can use the XC95288XL or the XC2C256 CPLD device.
- **Flash memory**: Used to store FPGA hardware and firmware image. It is usually divided into four areas
  - Factory default hardware sector: Used to store known good data and reconfigure the FPGA if the hardware update fails
  - Factory default software sector
  - Hardware update sector. After power up, the CPLD gets the FPGA bit stream data from this sector and tries to configure the FPGA three times. If this fails or results in a software loading timeout, then the CPLD sets the Flash bank address (2-bit MSB) to the factory default area (known good data) and reverts to the previous FPGA configuration
  - Software update sector
- **Ethernet PHY device**