Simplified Programming of Xilinx Devices Using a SCANSTA111/112 JTAG Chain Mux

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The SCANSTA111/112 Provides a Straightforward and Flexible Method of Isolating Scan Chains for Simplified Programming

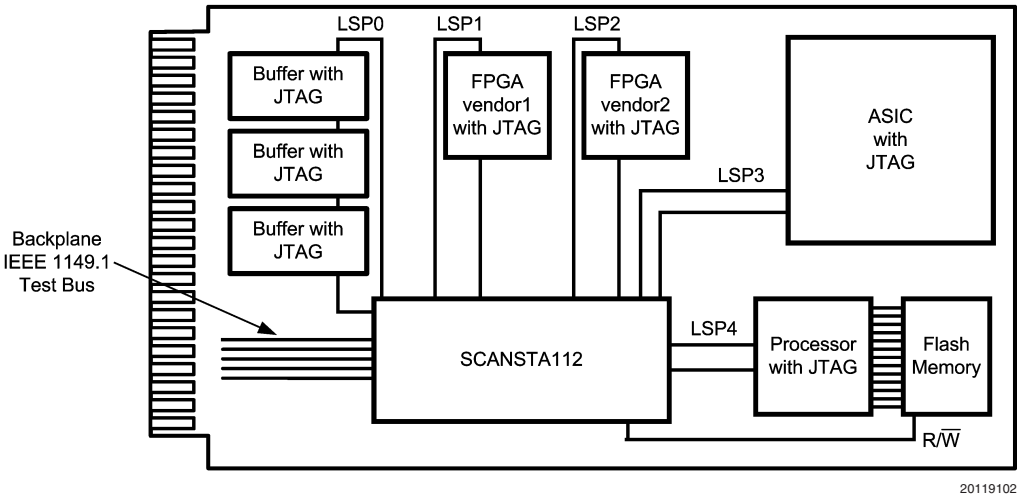
Many modern communication and networking systems incorporate a system-wide IEEE 1149.1 (JTAG) test bus infrastructure. This test bus not only enables a comprehensive life-cycle approach to system test, but it also offers a number of additional benefits to the system designer as the utility of the JTAG bus continues to expand beyond the boundaries of just test. JTAG is now used for emulation, memory programming, and configuration of CPLD's or FPGA's, and these approaches are well supported by the industry.

As the JTAG test bus infrastructure expands within a circuit board or system, the need to manage the JTAG bus becomes apparent. Grouping similar technologies into smaller, local scan chains can reduce complexity and improve debug and fault isolation. Partitioning particular components onto an individual scan chain maximizes access for speed-critical applications, such as configuring large/multiple CPLD's or FPGA's. Systems with multiple cards and complex backplanes continue to utilize the JTAG infrastructure on each circuit card by extending the JTAG test bus across the backplane. Multiple cards can share the test bus when each card utilizes a JTAG interface device that enables multidrop JTAG.

National's SCANSTA111 and SCANSTA112 devices (STA11x) enable a backplane test bus and partitioning of scan chains. Each device supports a multidrop addressable backplane, and manages up to 3 or 7 local scan chains (respectively). The STA11x are commonly used for isolating components on a circuit board, particularly when configuring CPLD's or FPGA's.

When developing configuration vectors for Xilinx CPLDs, FPGAs and PROMs, physically adding the STA11x into the scan path introduces a new device that the Xilinx iMPACT programming tool is not expecting. For some STA11x operating modes, the Xilinx iMPACT tool can provide a SVF (Serial Vector Format) file that may be modified in order to access the target device through the STA11x. This SVF may then be played through various means (e.g. stand alone Xilinx XSVF player from XAPP058, System ACE CF, or third-party JTAG tools).

In order to configure a Xilinx ISP device, there are a couple simple additional steps needed, and the following provides a basic description of how to accomplish this.



Typical use of SCANSTA112 to manage multiple JTAG chains on a single board

SCANSTA111/112 Operating Modes

There are three basic ways to get "through" the STA11x devices: Transparent Stitcher Mode, Transparent ScanBridge Mode, and Normal ScanBridge mode.

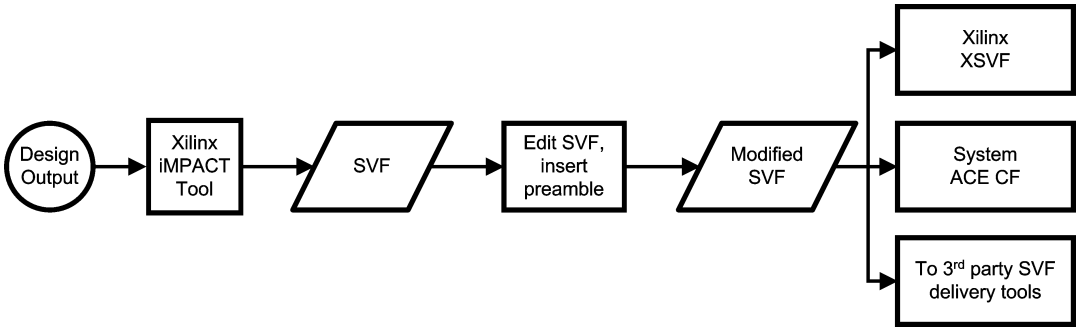
Transparent Stitcher Mode (STA112 feature only) is activated by way of external pins, and does not require changes to the SVF, but does require external hardware control. SB/S = 0 selects the Stitcher mode, TRANS will put the device into transparent mode, and the LSP select pins are used to select the appropriate LSP.

Transparent Stitcher Mode is specifically recommended when configuring Xilinx FPGAs due to bitstream alignment requirements of the Xilinx FPGA.

Transparent ScanBridge Mode requires a preamble in the vectors that are used to configure the Xilinx ISP devices. The iMPACT tool can also write out an SVF file that can be "played" later by third party SVF deliver tools to do the actual configuration. Note that when the STA11x is in transparent mode it is simply buffering the dot1 signals. Therefore, it is adding delay and may require that the clock speed be lowered. Examples 1 and 2 below demonstrate preambles to configure the STA11x device into Transparent ScanBridge Mode. Once this is executed, the STA11x device acts as a set of buffers between the backplane side and the LSP side of the device (i.e.; Tester TDO → STA11x TDI → STA11x LSP TDO → local chain → STA11x LSP TDI → STA11x TDO → Tester TDI).

Normal ScanBridge Mode also requires a preamble in the vectors used to configure a Xilinx ISP device. Note, however, that when the STA11x is not in transparent mode, it adds a re-synchronization bit (PAD-bit) to the end of the chain. This re-times the signals and allows for a clock speed equal to the original, but requires the addition of the pad bit into the scan path for each LSP inserted in the path. Examples 3 and 4 below demonstrate preambles to configure the device into normal ScanBridge Mode. Once this is executed, the STA11x acts as a set of buffers between the backplane side and the LSP side of the device, with the addition of the pad bits (i.e.; Tester TDO → STA11x TDI → STA11x LSP TDO → local chain → STA11x LSP TDI → PAD-bit → STA11x TDO → Tester TDI). Note that this will require additional bits in the scan process for the register and the pad-bits.

In complex ScanBridge architectures, PAD-bits that are put inline prior to the FPGA might misalign critical bitstream data arriving at the FPGA. This method is not recommended for configuring Xilinx FPGA devices.



Tool chain and process for modifying SVF

Example code from Xilinx Modified SVF

The following section of code is modified SVF from the iMPACT tool output. In this example we have an STA11x device at hex address (1B) and the target device is located on LSP1. In the example below we have added two lines of code (lines 6 and 7) that address the correct device and select the correct local port.

```
// Created using Xilinx iMPACT Software [ISE Foundation - 6.3.01i]
TRST OFF;
ENDIR IDLE;
ENDDR IDLE;
STATE RESET IDLE;
```

SIR 8 TDI(1B); ! <<<-- level one protocol, STA11x at address 1B hex

SIR 8 TDI(A1); ! <<<-- level two protocol, target device on LSP 1

```
TIR 0; !
HIR 0; ! Describes additional devices in the chain besides the target device
TDR 0; !
HDR 0; !
// Validating chain...
HIR 0 ;
TIR 0 ;
TDR 0 ;
HDR 0 ;
SIR 8 TDI (ff) SMASK (ff) TDO (01) MASK (e7) ;
//....rest of SVF file
```

Example Code for Simulations and Verification

TRANSPARENT SCANBRIDGE MODE

For the first example, let's assume the STA11x is at address (11) and the target device is located on LSP0. In example 2, we assume the STA11x is at the same address but the target device is on LSP1.

Example 1: Configuring an LSP of the STA11x in Transparent ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Address ScanBridge
SIR 8 TDI (A0); ! Load instruction to enable transparent mode for LSP0
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (C3); ! Try to load GOTOWAIT in ScanBridge
SDR 8 TDI (5a); ! Verify that ScanBridge did not recognize GOTOWAIT
! Now TDIB → lsp0 → TDOB
```

Example 2: Configuring an LSP of the STA11x in Transparent ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Address ScanBridge
SIR 8 TDI (A1); ! Load instruction to enable transparent mode for LSP1
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (C3); ! Try to load GOTOWAIT in ScanBridge
SDR 8 TDI (5a); ! Verify that ScanBridge did not recognize GOTOWAIT
! Now TDIB → lsp1 → TDOB
```

NORMAL SCANBRIDGE MODE

For example 3, we assume the STA11x is at address (01) and LSP's 0, 1, and 2 will be connected to the backplane port. In example 4, we assume the STA11x is at the same address (01) but only LSP0 is connected to the backplane port.

Example 3: Configuring LSP's of the STA11x in "normal" ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI(01); ! scan in address
SIR 8 TDI(8E); ! modesel-0 Setup mode register to select LSP
SDR 8 TDI(07); ! LSP0-2 STA11x
SIR 8 TDI(E7); ! UNPARK Sync LSPs to backplane port.
! MR0: X000X111
! TDIB → register → lsp0 → pad → lsp1 → pad → lsp2 → pad → TDOB
```

Example 4: Configuring LSP's of the STA11x in "normal" ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI(01); ! scan in address
SIR 8 TDI(8E); ! modesel-0 Setup mode register to select LSP
SDR 8 TDI(01); ! LSP0 STA11x
SIR 8 TDI(E7); ! UNPARK Sync LSPs to backplane port.
! MR0: X000X001
! TDIB → register → lsp0 → pad → TDOB
```

Notes

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