An LDO Primer

Part II: A Review on Regulation, Stability and Compensation

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In Part I of this article series, we reviewed factors that determine the dropout voltage, ground current and output current of a linear regulator. In this article, we will discuss the operational imperative of the linear regulator: stable regulation of the output voltage. Many editorials have discussed this issue in the past (see references 1 and 2). This article provides a practical, straightforward look at LDO regulation, stability, and compensation, including equations and illustrations userful to design engineers of many different experience and education levels.

First, let us review the three key elements of a "generic" linear regulator:

1. A pass element
2. A band gap voltage reference
3. An error amplifier

The output voltage regulation of the linear regulator is achieved by feedback. To illustrate the feedback concept, let us use the PNP pass transistor regulator as an example (Figure 1.a, without the coupling transformer).

The resistor divider, error amplifier, and pass element of the PNP pass transistor regulator form a *closed loop*. The output voltage, V_{OUT}, provides a feedback voltage through the resistor divider, $V_C = V_{OUT} * R2/ (R1 + R2)$, to the non-inverting input of the error amplifier. The band gap reference output (V_{REF}) is a high-precision, fixed voltage that is tied to the inverting input of the error amplifier. The error amplifier, essentially an op amp, then makes V_C equal to V_{REF} by sourcing a ground current to the base of the PNP transistor. The PNP transistor, in turn, supplies sufficient output current to keep V_{OUT} at a certain value. A fraction of this value, V_C, is equal to V_{REF}. The regulated output voltage, therefore, is defined as:

$$V_{OUT} = V_{REF} X (1 + R1/R2) \quad (1)$$

This equation illustrates that the feedback is negative, and the adjustment of the output voltage resulting from the feedback is in opposite polarity to the "original" change on the output voltage. In real-life applications, sufficient negative feedback is required for a closed loop to remain stable.

For example, imagine that a small disturbance is introduced to the loop. The coupling of a small sinusoidal signal to the PNP pass transistor regulator through a transformer models this disturbance (Figure 1.a).

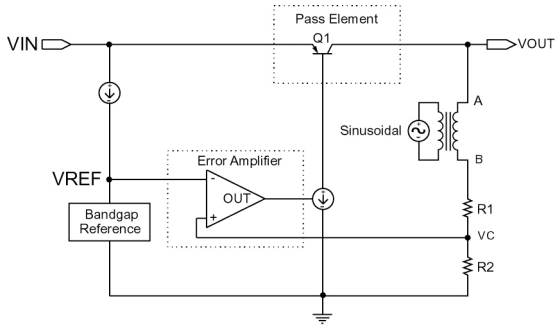

Figure 1a

Figure 1.a – Closed Loop Phase Shift Model

Initially, the small signal has a value of ΔV_A at point A, and a value of ΔV_B at point B. The signal at point B then travels through the loop and eventually arrives at point A, with a value of ΔV_B'. Although ΔV_A and ΔV_B' have the same magnitude, there is a difference in phase (in degrees) between the two.

To simplify our analysis, it is reasonable to establish that the error amplifier introduces a "perfect" negative feedback to the loop. That is, if there were only the error amplifier in the feedback loop, ΔV_A would lag ΔV_B' by -180° (Figure 1.b). However, because of the pass element's built-in capacitance, it introduces a phase shift that reduces the perfect -180° phase difference by a value between 0° and -180° (counter-clockwise, with -180° as the starting point).

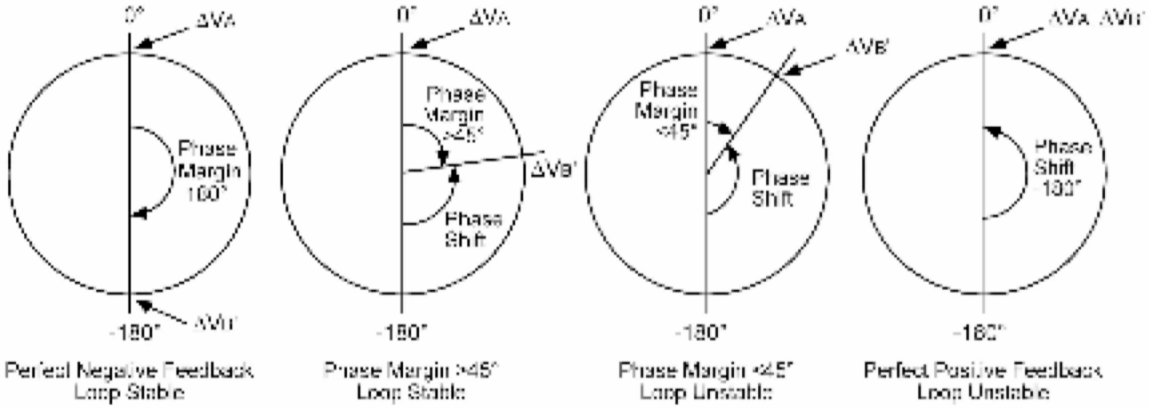

FIGURE 1.b - Closed Loop Stability Map

Figure 1.b – Closed Loop Stability Map

At this point, it is fitting to introduce the *Bode plot*, a simple yet effective tool that is widely used to analyze closed loop stability. A Bode plot includes a loop gain curve and a phase shift curve. These curves track the movements of poles and zeros created by the impedances of the components that form the loop. The behaviors of the poles and zeros determine the loop stability. A pole decreases the loop gain slope by -20dB/decade at its pole frequency, f_P. It also introduces a -90° phase shift (counter clockwise) from the frequency one decade below f_P (f_P/10) to the frequency one decade above f_P (10f_P), with a -45° phase shift at f_P (Figure 2.a). Both loop gain slopes decrease and phase shifts are additive, meaning that each additional pole decreases the loop gain slope by another -20dB/decade, and increases the phase shift by an additional -90°. An RC pair in low-pass filter configuration models a pole (Figure 2.b), with its f_P defined as:

$$f_P = 1/2\pi RC, \text{ expressed in Hz} \qquad (2)$$

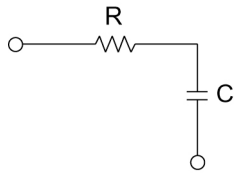

Figure 2a

Figure 2.a – Pole: RC Low-Pass Filter

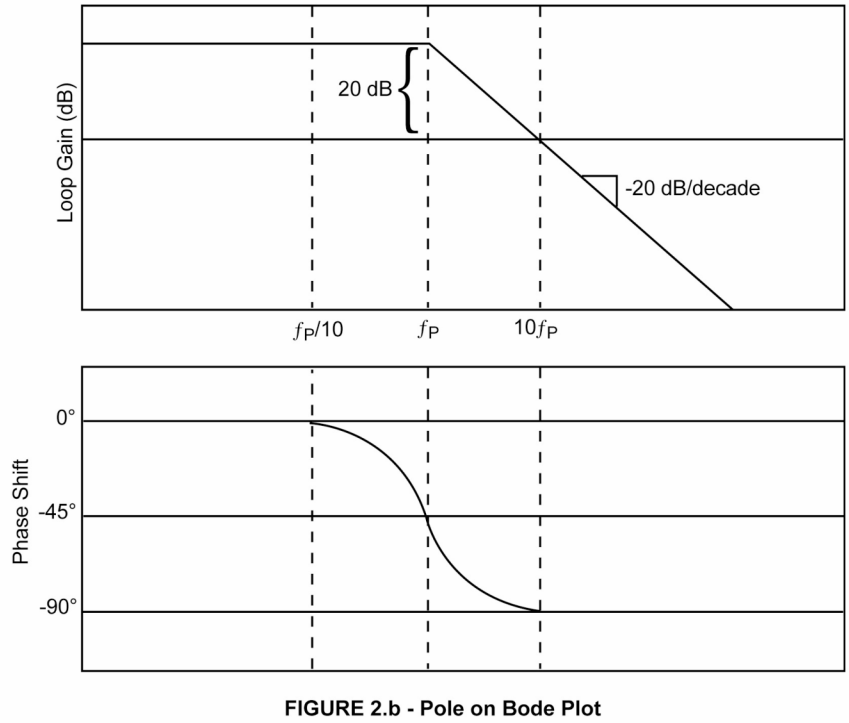

FIGURE 2.b - Pole on Bode Plot

Figure 2.b – Pole on Bode Plot

A zero, on the other hand, increases the loop gain slope by +20dB/decade at its zero frequency (f_Z). It also introduces a +90° phase shift (clockwise) from the frequency one decade below f_Z ($f_Z/10$) to the frequency one decade above f_Z ($10f_Z$), with a +45° phase shift at f_Z (Figure 3.a).

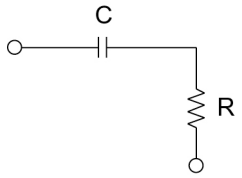

Figure 3a

Figure 3.a – Zero: RC High-Pass Filter

Loop gain slope increase and phase shift created by a zero are also additive. An RC pair in high-pass filter configuration (Figure 3.b) with its f_Z shown by the following equation models a zero:

$$f_Z = 1/2\pi RC, \text{ expressed in Hz} \qquad (3)$$

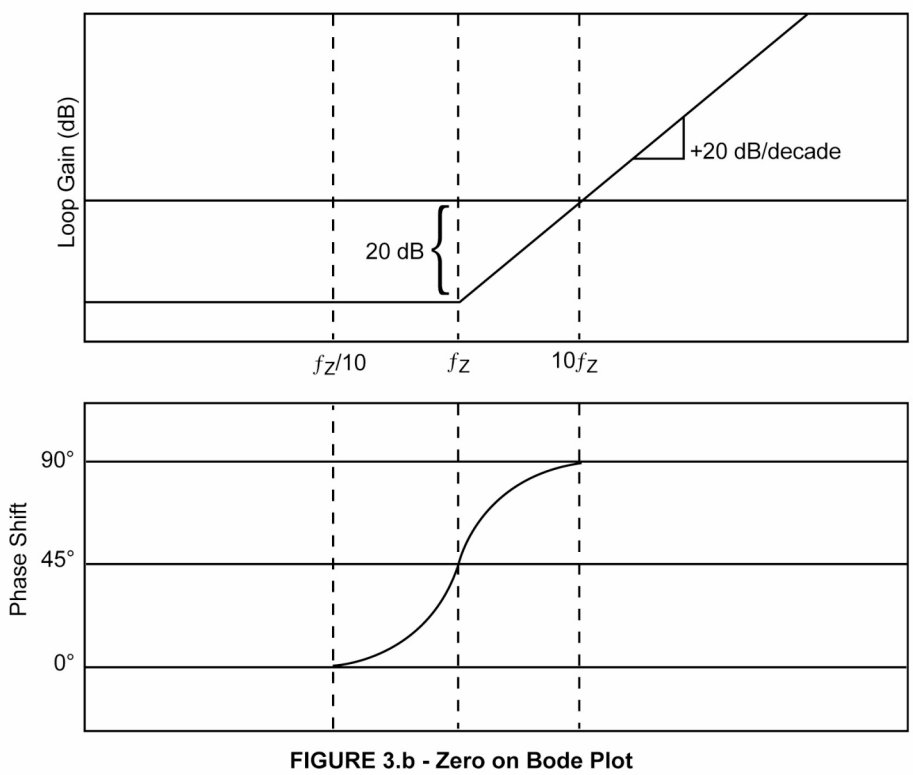

FIGURE 3.b - Zero on Bode Plot

Figure 3.b – Zero on Bode Plot

In our example (Figure 1.a), the loop gain (A) of the closed loop is given as:

$$A = 20\log(|V_A/V_B|), \text{ expressed in dB} \quad (4.a)$$

The single most important stability indicator of a closed loop is phase margin, defined as the difference (expressed in degrees) between -180° and the total phase shift of the loop at the frequency where the loop gain is 0dB (unity gain). Phase margin is a positive number (clockwise) between 0° and 180°, and is expressed as:

$$\Phi = 180° + \text{phase shift} \quad (4.b)$$

*where phase shift is a negative number (counter clockwise) between 0° and -180°

To keep the loop stable, it is a “rule of thumb” that the phase margin be no less than 45° (Figure 1.b). If a 45° phase margin cannot be achieved by the intrinsic architecture of the linear regulator, some form of compensation, either internal or external, is required.

We are now equipped to analyze the loop stability of linear regulators. We start with the standard NPN regulator (Figure 4.a).

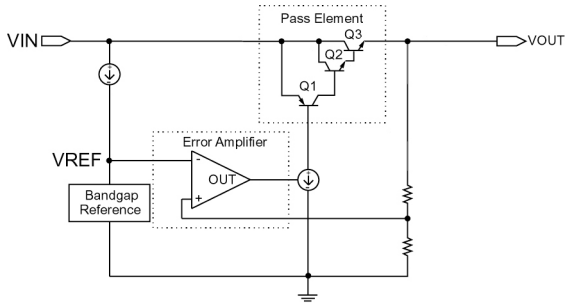

Figure 4a

Figure 4.a – Standard NPN Regulator

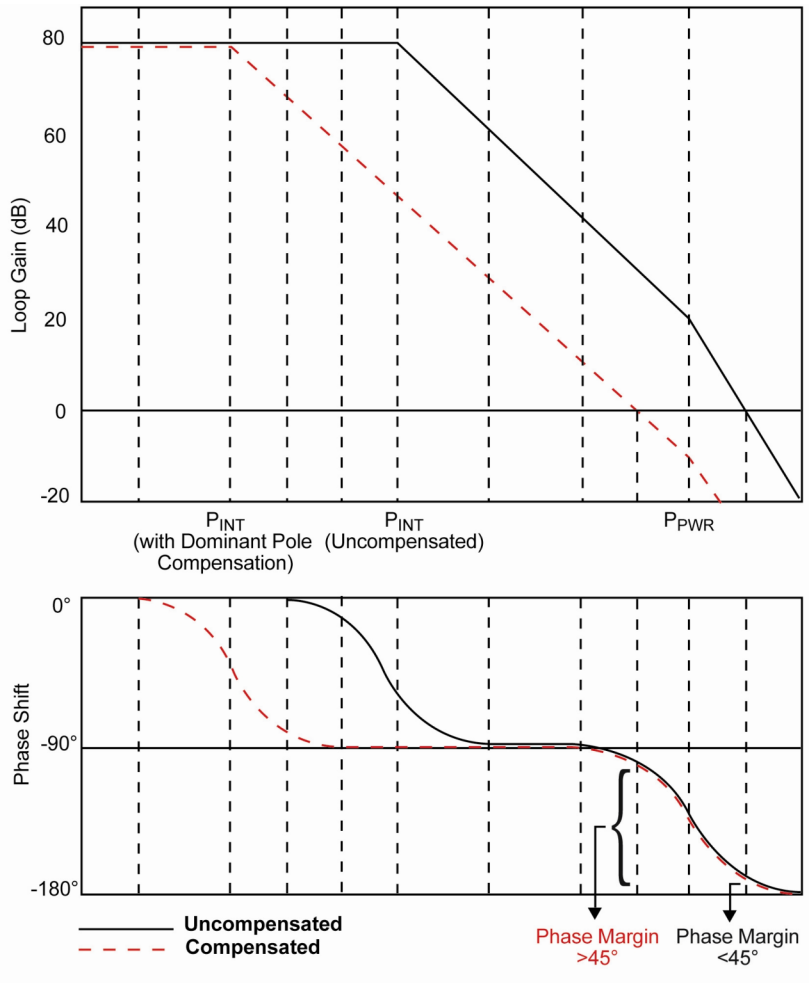

FIGURE 4.b - Bode Plot
(Uncompensated and Compensated)

Figure 4.b – Bode Plot

There are two poles in the standard NPN regulator -- a dominant pole (P_{INT}), created by the intrinsic capacitance of the regulator, and a power pole (P_{PWR}), created by the pass element. P_{INT} and P_{PWR} occur at the following frequencies:

$$f(P_{INT}) = 1/2\pi R_{INT}C_{INT} \quad (5.a)$$

*where R_{INT} and C_{INT} are the regulator's intrinsic resistance and capacitance

$f(P_{PWR}) = 1/2\pi R_{PWR}C_{PWR}$ (5.b)

*where R_{PWR} and C_{PWR} are the pass element's resistance and capacitance

As the NPN Darlington pair is in a common collector configuration, its output impedance is very low (i.e., $R_{PWR}C_{PWR}$ is very low). Therefore, P_{PWR} occurs at a very high frequency (Equation 5.b). On the contrary, P_{INT} occurs at a lower frequency because of the regulator's relatively high capacitance (Equation 5.a).

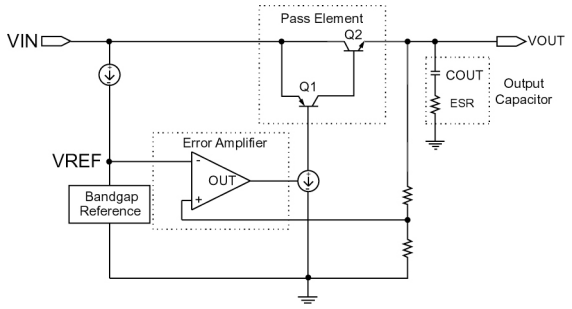

Figure 5a

Figure 5.a – NPN Pass Transistor Regulator

Still, P_{PWR} can occur at a frequency below 0dB crossover point, which may create a less than 45° phase margin. Thus, the loop can become unstable, which creates a need for compensation (Figure 4.b).

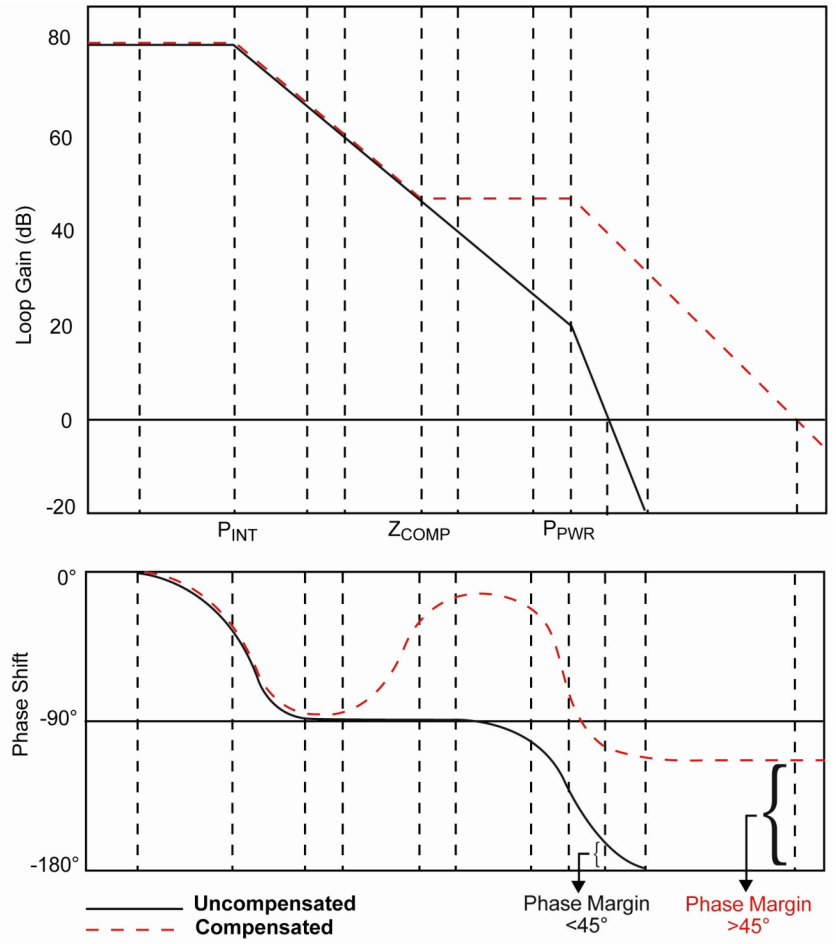

FIGURE 5.b - Bode Plot
(Uncompensated and Compensated)

Figure 5.b – Bode Plot

The standard NPN regulator employs an internal compensation scheme known as *dominant pole compensation*. Dominant pole compensation is achieved by adding intrinsic capacitance to the regulator. This additional capacitance moves P_{INT} to an even lower frequency (Equation 5.a) with no effect to $P_{PWR,}$ enabling it to occur at a frequency above the 0dB crossover point. The phase margin is now greater than 45°, resulting in a stable loop. As such, the standard NPN regulator is stable without external compensation (Figure 4.b).

The NPN pass transistor regulator (Figure 5.a) also has a dominant pole (P_{INT}) and a power pole (P_{PWR}). Like the standard NPN regulator, the NPN pass transistor is in common collector configuration with low output impedance. However, the NPN transistor is driven by a PNP transistor with high impedance. The net effect is that its output impedance, although high in comparison to other types of linear regulators, is not as high as that of the standard NPN regulator. Therefore, P_{PWR} occurs at a frequency lower than in the standard NPN regulator, and is usually below the 0dB crossover point. The result is a less than 45° phase margin, where compensation is needed to keep the loop stable (Figure 5.b).

Because of the relatively low frequency of P_{PWR}, the NPN pass transistor regulator cannot be stabilized by dominant pole compensation alone. Instead, a zero must be placed between P_{INT} and P_{PWR} to increase the phase margin to at least 45° (Figure 5.b). This is accomplished by using an external compensation method, such the addition of an output capacitor next to V_{OUT}. The frequency of the added zero (Z_{COMP}) is defined by:

$$f(Z_{COMP}) = 1/(2\pi \text{ X ESR X } C_{OUT}) \quad (6)$$

*where ESR is Equivalent Series Resistance of the output capacitor

Because P_{PWR} of the NPN pass transistor regulator still occurs at a still rather high frequency, output capacitor selection is fairly easy. As long as $f(Z_{COMP})$ is lower than $f(P_{PWR})$, C_{OUT} can be small, and ESR is not critical.

The PNP pass transistor regulator (Figure 6.a), on the other hand, requires more careful selection of an output capacitor. Its pass element, the PNP transistor, is in a common emitter configuration, which exhibits high output impedance. This is important on two fronts:

1. P_{PWR} occurs at a frequency lower than in the NPN pass transistor regulator.
2. The impedance of the load, created by load resistance and output capacitance, becomes a significant contributor to loop stability by adding another low frequency load pole (P_L) to the Bode plot. The frequency of P_L is expressed as:

$$f(P_L) = 1/(2\pi R_{LOAD}C_{OUT}) \quad (7)$$

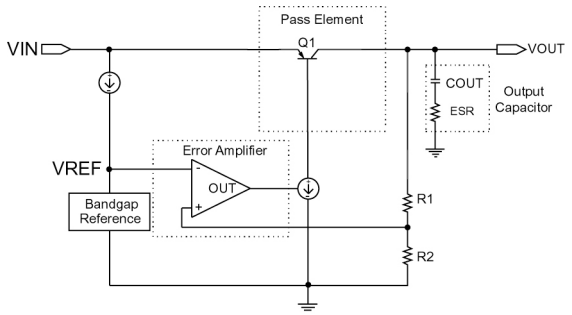

Figure 6a

Figure 6.a – PNP Pass Transistor Regulator

Typically, R_{LOAD} and C_{OUT} are higher than the regulator's intrinsic resistance (R_{INT}) and capacitance (C_{INT}), which makes P_L occur at a frequency lower than $f(P_{INT})$. It is immediately obvious that the PNP pass transistor regulator is not stable, even with dominant pole compensation (Figure 6.b). A zero must be added to compensate for this instability. Again, this is accomplished by the addition of an output capacitor next to V_{OUT}.

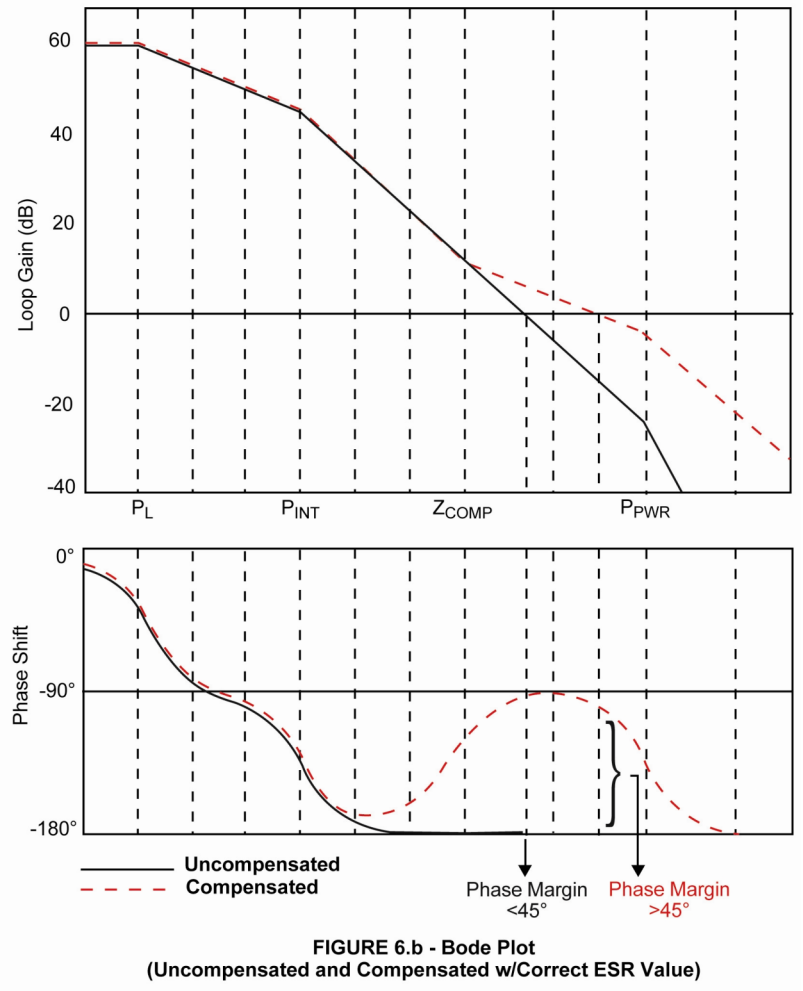

Figure 6.b – Bode Plot

Further, where the zero is placed in the frequency space is critical. The placement location of the zero translates to a careful matching of the output capacitor's capacitance and ESR.

The zero must occur somewhere between P_{INT} and P_{PWR} (Figure 6.b). Because P_{PWR} occurs at a relatively low frequency, the "space" between P_{INT} and P_{PWR} is narrow; hence, the choice of $f(Z_{COMP})$ is narrow and is demonstrated as:

$$f(P_{INT}) < f(Z_{COMP}) < f(P_{PWR})/10 \quad (8)$$

Equation 8 illustrates the "rule of thumb" that Z_{COMP} must occur above $f(P_{INT})$, and at least one decade below $f(P_{PWR})$. This is because Z_{COMP} needs the full one decade above $f(Z_{COMP})$ to fully realize its +90° phase shift. As Equations 5.a, 5.b, 6, and 8 show, for loop stability at any given capacitance value, the ESR has to satisfy the following:

$$R_{INT}C_{INT}/C_{OUT} > ESR > 10R_{PWR}C_{PWR}/C_{OUT} \quad (9)$$

If the ESR is either too high or too low, it is out of range.

The ESR is too high when the following condition exists:

$$ESR > R_{INT}C_{INT}/C_{OUT} \quad (10)$$

Under this condition, Z_{COMP} occurs at a frequency below $f(P_{INT})$ (Figure 6.c). Because of the narrow space between P_L and P_{INT}, Z_{COMP} can be within one decade of $f(P_{INT})$. This prevents Z_{COMP} from realizing its full +90° phase shift. As a result, the phase margin may not rise above 45°; hence, the loop remains unstable.

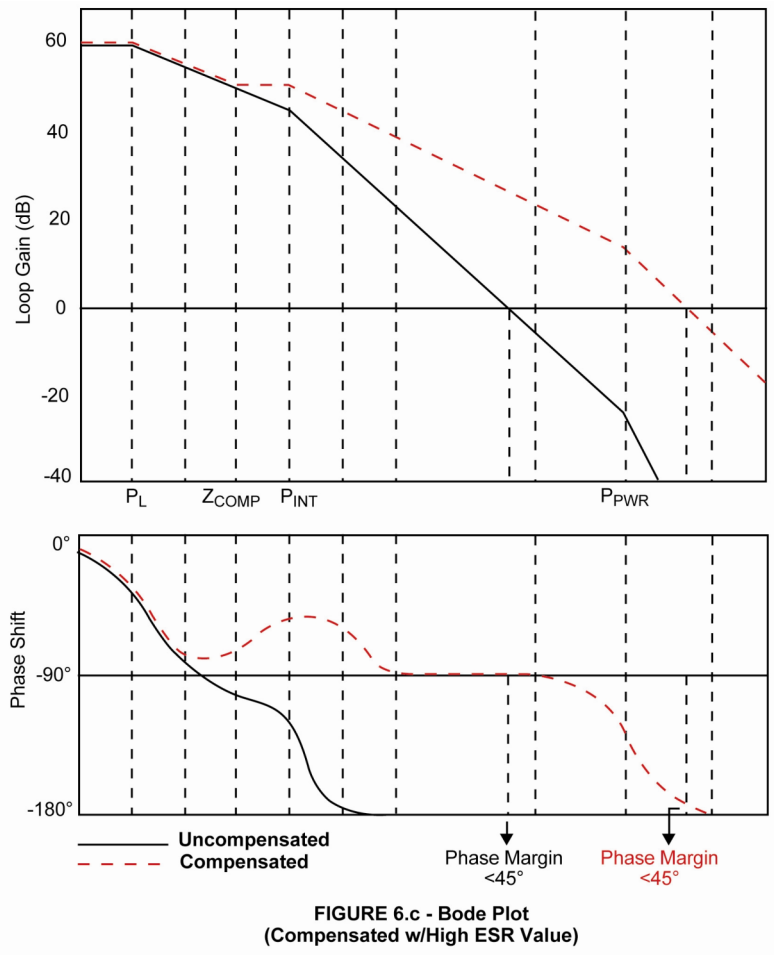

FIGURE 6.c - Bode Plot
(Compensated w/High ESR Value)

Figure 6.c – Bode Plot

On the other hand, ESR is too low when the following is true:

$$ESR < 10R_{PWR}C_{PWR}/C_{OUT} \quad (11)$$

Here, Z_{COMP} occurs within one decade below $f(P_{PWR})$, which prevents it from realizing its full +90° phase shift (Figure 6.d). Therefore, the phase margin will not rise above 45°, and the loop, again, remains unstable.

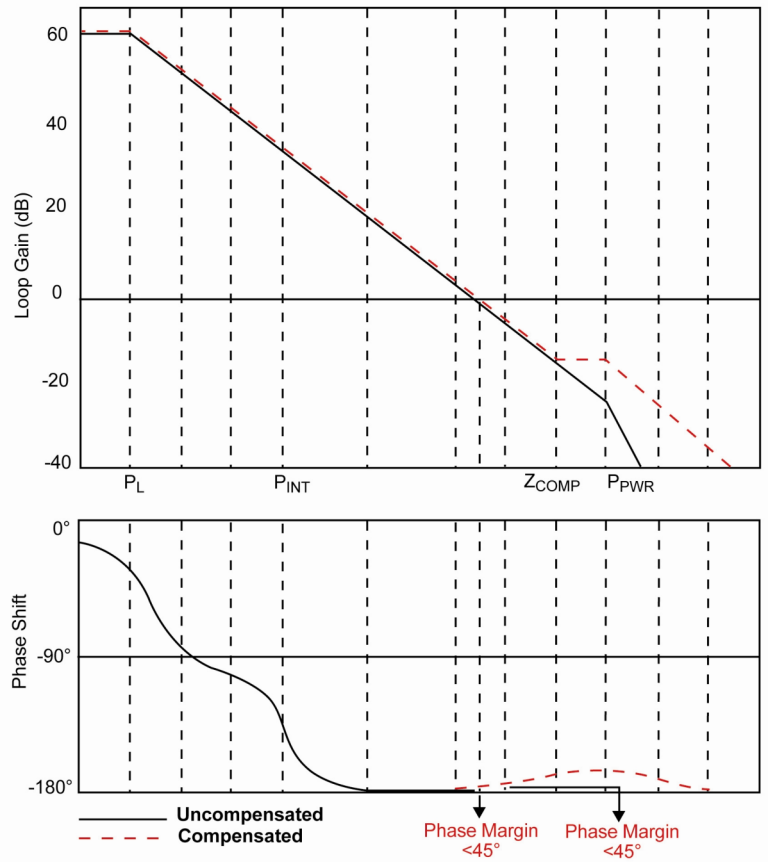

FIGURE 6.d - Bode Plot
(Compensated w/Low ESR Value)

Figure 6.d – Bode Plot

The P-channel FET regulator (Figure 7.a) has its pass element (the P-channel FET) in a common source configuration, similar to a PNP transistor in a common emitter configuration with relatively high output impedance. As such, the P-channel FET regulator has loop stability behavior similar to the PNP pass transistor regulator. The P-channel FET regulator, therefore, requires a carefully selected output capacitor to keep the loop stable (Figure 7.b).

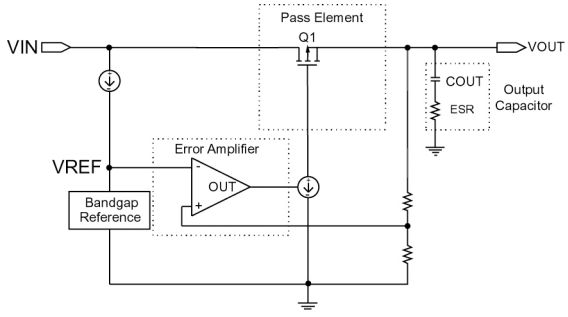

Figure 7a

Figure 7.a – P-channel FET Regulator

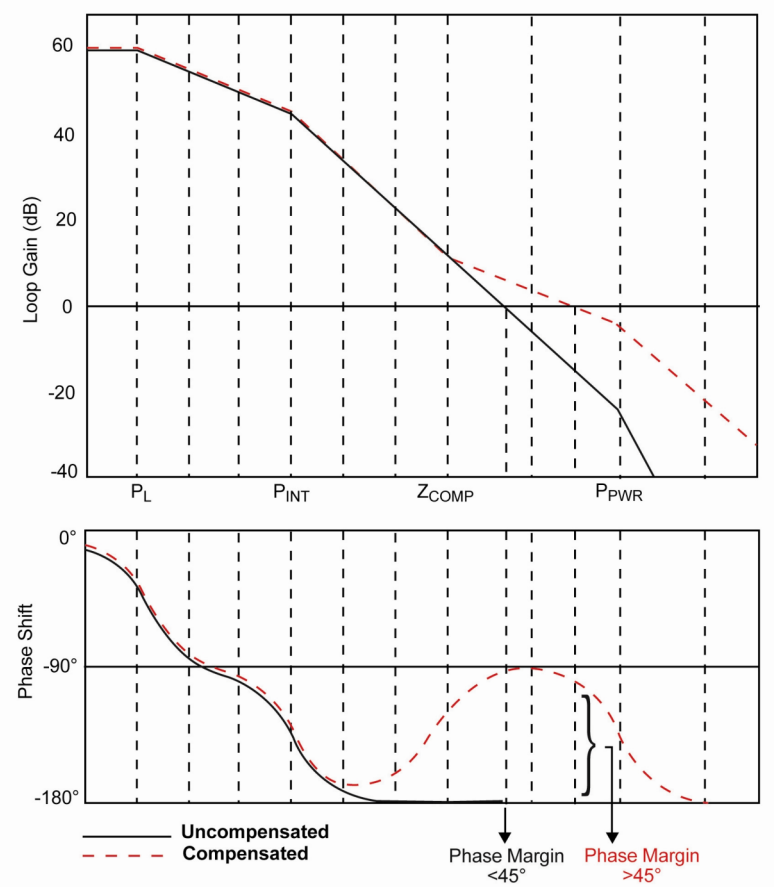

FIGURE 7.b - Bode Plot
(Uncompensated and Compensated w/Correct ESR Value)

Figure 7.b – Bode Plot

Finally, the N-channel FET regulator (Figure 8.a) has its pass element (the N-channel FET) in a common drain configuration similar to an NPN transistor in a common collector configuration. In reality, the N-channel FET regulator's output impedance is not as low as that of the standard NPN regulator. Rather, it is comparable to that of the NPN pass transistor regulator. There, the N-channel FET regulator exhibits similar loop stability behavior to the NPN pass transistor regulator, which requires an output capacitor for stability compensation. However, in this case, the ESR of the output capacitor is not as critical (Figure 7.b).

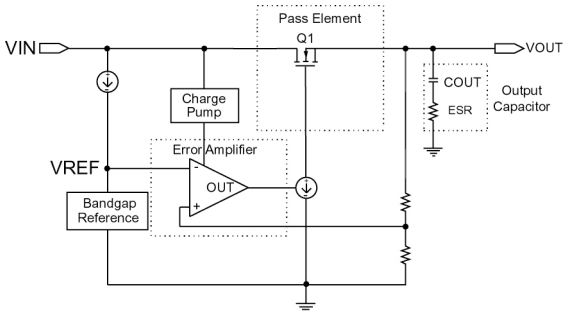

Figure 8a

Figure 8.a – N-channel FET Regulator

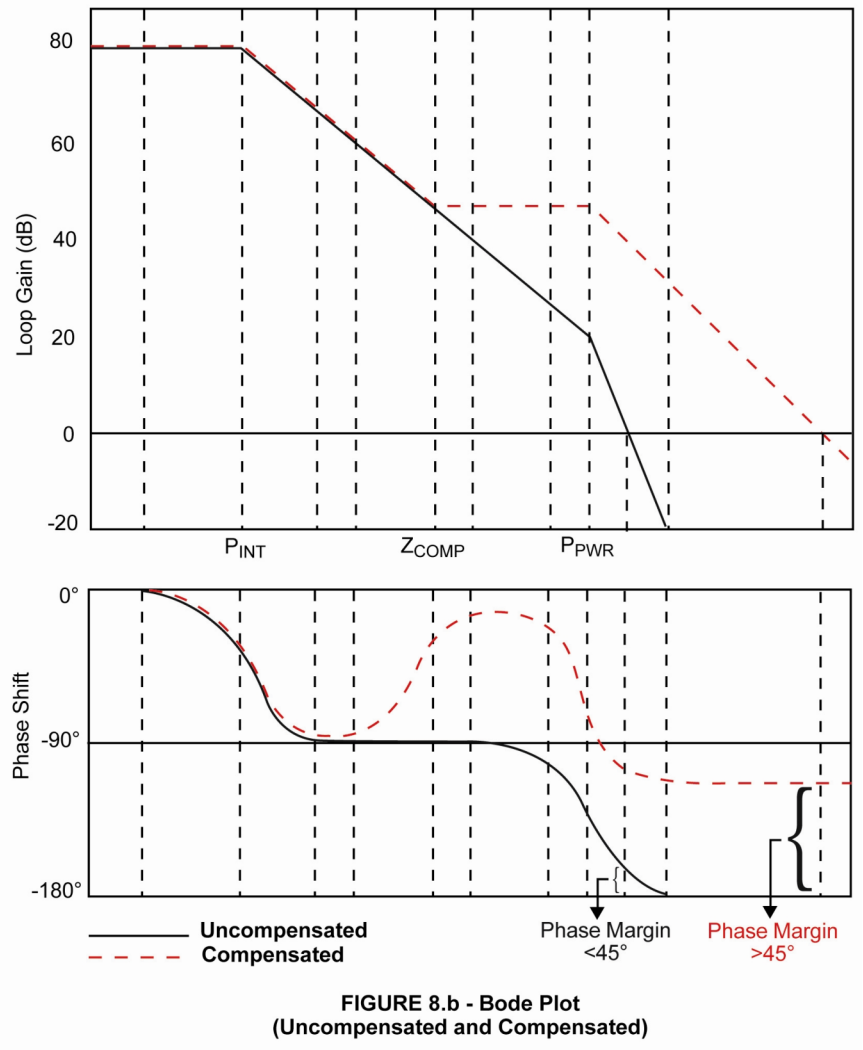

FIGURE 8.b - Bode Plot
(Uncompensated and Compensated)

Figure 8.b – Bode Plot

In conclusion, the Bode plot is an effective tool for analyzing closed loop stability of linear regulators. Phase margin is the most important indicator of stability. If a greater than 45-degree phase margin cannot be achieved by the intrinsic architecture of the linear regulator, an internal or external compensation method, such as an output capacitor, can be used to ensure closed loop stability. The following table summarizes the loop stability characteristics and compensation methods for each of the linear regulators.

References:

1. "Linear Regulators: Theory of Operation and Compensation," Simpson, Chester, May 2000,

Regulator Type	Standard NPN (Darlington)	NPN Pass Transistor	PNP Pass transistor	P-channel FET	N-channel FET
Pass Element Configuration	Common Collector (Emitter Follower)	Common Collector (Emitter Follower)	Common Emitter	Common Source	Common Drain
Output Impedance	Very Low	Low	High	High	Low
Compensation Required	Internal	Internal and External	Internal and External	Internal and External	Internal and External
Compensation Scheme	Dominant Pole Compensation	External Output Capacitor	External Output Capacitor	External Output Capacitor	External Output Capacitor
Output Capacitor ESR	N/A	Not Critical	Within Certain Range	Within Certain Range	Not Critical

National Semiconductor Application Note 1148

2. "Art of Electronics," Horowitz, Paul and Hill, Winfield, Cambridge University Press, 2nd Edition (July 1989), Chapter 2 (Section 2.04), Chapter 3 (Section 3.08), Chapter 4 (sections 4.33, 4.34, 4.35)