



Virtex-6 and Spartan-6 FPGA Families Frequently Asked Questions

XILINX UNVEILS NEXT GENERATION FPGA FAMILIES

GENERAL

1. What is Xilinx announcing today?

- The introduction of the high-end Virtex®-6 and low-cost Spartan®-6 FPGA families, the next generation in FPGAs from Xilinx. These two new FPGA families serve as the foundation for targeted design platforms that enable software and hardware designers alike to leverage common design methodologies, development tools, and run-time platforms. This allows them to spend less time developing the infrastructure of an application and more time building differentiating features into the end application.

2. What is a targeted design platform, and how is it different from the domain-optimized FPGA platform you introduced with the Virtex®-5 FPGA family?

- Targeted design platform is a Xilinx-specific term that describes the integration of five key components with customer design process and success in mind: 1) FPGA devices, 2) intellectual property (IP) cores, 3) design environments with industry-proven methodologies, 4) robust reference designs, and 5) scalable boards and kits. With FPGAs delivered by Xilinx, each of the components may be delivered by either Xilinx or third parties.
- FPGA Platform is a Xilinx term used to describe a set of FPGA devices optimized to address the needs of certain application areas or domains, such as DSP, connectivity, and embedded processing. For example, Virtex-6 SXT FPGA Platform is optimized for DSP designs.

3. What are the key capabilities and features of the Virtex-6 and Spartan-6 FPGA Families?

- The Virtex-6 FPGA family is the sixth generation in the Virtex FPGA Series. Virtex-6 FPGAs are fabricated on a high-performance, 40-nanometer (nm), triple-oxide, 12-metal layer process using 300mm wafers. These devices operate on 1.0v core voltage. A 0.9v low power option is also available. Xilinx built this new family of devices using the third generation of the company's proprietary ASMBL™ architecture and offers three domain-optimized platforms (sub-families) to deliver different feature mixes to best address a variety of customer applications:



all-electronics.de
ENTWICKLUNG. FERTIGUNG. AUTOMATISIERUNG



Entdecken Sie weitere interessante Artikel und News zum Thema auf all-electronics.de!

Hier klicken & informieren!



Virtex-6 and Spartan-6 FPGA Families -- Frequently Asked Questions

- Virtex-6 LXT FPGAs: optimized for applications that require high performance logic, DSP, and serial connectivity
 - Virtex-6 SXT FPGAs: optimized for applications that require ultra-high performance DSP and serial connectivity
 - Virtex-6 HXT FPGAs: optimized for communications applications that require the highest speed serial connectivity
- The sixth generation in the Spartan FPGA Series, the Spartan-6 FPGA family is fabricated on a mature, low-power 45nm, 9-metal layer dual-oxide process technology. The new low-cost family delivers the optimal balance of cost, power, and performance by utilizing new, more efficient dual-register 6-input LUT logic for higher system performance, as well as a rich selection of built-in system-level blocks including memory controllers, DSP and PCI® Express. Spartan-6 FPGAs also come with advanced power management capabilities with the ability to operate at a lower power 1.0v core option. The family is delivered on two FPGA platforms:
 - Spartan-6 LX FPGAs: cost-optimized logic, memory and DSP
 - Spartan-6 LXT FPGAs: LX features plus high speed transceivers
 - Together, the new families offer 20% faster performance, at 40% lower cost and up to 65% less power consumption. The new process geometries enable greater than 200% the logic capacity and greater than 300% register density as previous families. The Virtex-6 and Spartan-6 Families also offer greater than 200% DSP bandwidth, greater than 200% higher serial IO bandwidth, and greater than 37% higher parallel IO bandwidth. With increased I/O bandwidth, FPGA designers can utilize DDR3 and higher I/O transfer rates to complement the higher performance from the FPGA itself.
- 4. When will Virtex-6 and Spartan-6 FPGAs be available, and how much will they cost?**
- Spartan-6 devices are sampling to customers today with general availability of both families in CY Q3. Software support is available now for customers in the Early Access Program. Customers can contact their Xilinx sales representative to discuss volume pricing.
 - The first Virtex-6 device to be available will be the LX240T FPGA. This device offers the best migration possible to the entire family, meaning that from the LX240T FPGA designers can migrate to any other Virtex-6 device (with the exception of the LX760) by selecting the appropriate package.
- 5. Will the EasyPath™ program be available for Virtex-6 FPGAs and when?**
- Yes. Virtex-6 FPGAs will provide designers with the EasyPath option. The exact parts are determined, depending upon part size and quantity. The EasyPath program is expected to provide 30 to 75% cost reduction and will be available starting the first calendar year quarter of 2011.
- 6. What types of applications and end-markets do the new FPGA families support?**

Virtex-6 and Spartan-6 FPGA Families -- Frequently Asked Questions

- The Virtex-6 FPGA family leverages the Xilinx ASMBL architecture to provide a fine-tuned combination of resources that address high-performance digital signal processing common in compute-intensive infrastructure applications such as current and next-generation wireless radio and baseband processing. Wired telecom and data-comm routers, switches, bridges and aggregators require high speed programmability, the ability to partition designs into multiple clock domains, and the ability to route data using high-speed serial transceiver technology running either proprietary or standard interface protocols.
- The Spartan-6 FPGA family provides optimal system integration capabilities for many cost-sensitive applications. The 11-member device family delivers a density range from 4K to 150K logic cells, with half the power consumption, faster and more comprehensive connectivity, and significant ease-of-use improvements over alternative high volume FPGA platforms. Xilinx will introduce fully functional market-specific Spartan-6 FPGA platforms for automotive, consumer, and industrial among others, all designed to take advantage of the unique capabilities of the Spartan-6 FPGA platform.

7. What key customer benefits do the new platforms deliver?

- The focus on power efficiency has never been more important. Both Virtex-6 and Spartan-6 FPGA Families leverage innovative techniques to manage both static and dynamic power consumption with reductions greater than 65% as compared to previous families. Designers have the ability to control power consumption, while maintaining the flexibility to address their performance and density requirements.
- The combination of hard IP and programmability on the 40nm/45nm architectures lends itself to greater integration of system components, which helps to drive down the cost and complexity of systems. Designers can build high speed connectivity into their systems with built-in serial transceiver capabilities that are designed to bring systems together over a back plane, across fiber or copper, or chip-to-chip.
- For better productivity, Xilinx designed the Virtex-6 and Spartan-6 Families to allow migration of designs from previous generation Virtex and Spartan devices. Designers can also choose from over 100 IP cores and reference designs designed to work across the two new families.

8. What are the DSP capabilities of the two new families?

- The enhanced DSP48E1 slices in the Virtex-6 FPGA family and the 50% more DSP48A1 slices in the Spartan-6 FPGA family enable highly efficient, high performance implementation of DSP functions, such as filters as well as other commonly used mathematical and bit-manipulation functions.
- The Virtex-6 DSP slice is very similar to the Virtex-5 family DSP48E slice (25x18 multiplier with a second stage that can do accumulation as well as additions, subtractions, and logic functions). The main change is the addition of a pre-adder. The Virtex-6 pre-adder function is a performance and utilization enhancement, as

Virtex-6 and Spartan-6 FPGA Families -- Frequently Asked Questions

many Virtex-5 FPGA DSP customers were building pre-adder functionality in FPGA logic.

9. Why doesn't Xilinx offer a hard memory controller for Virtex-6 FPGAs while it will offer it for Spartan-6 product?

- The dynamics between Spartan markets and Virtex markets are quite different. Virtex devices are often connected to a wide set of memory interfaces (DDR2, DDR3, QDR, RLDRAM, etc.). Implementing a hard memory controller for Virtex-6 FPGAs to support all these memories would require a larger amount of dedicated silicon, which presents an unjustifiable cost for most applications. Therefore, the soft implementation of the exact memory controller required (DDR2, QDR, etc.) is a better choice.

10. What security mechanism will be available in Virtex-6 and Spartan-6 FPGAs?

- Virtex-6 FPGAs will support the same security options as Virtex-5 FPGAs: a 256-bit AES encryption mechanism relying on SRAM cells to store the key, maintained by a battery. This is the highest level of security that can be provided and complies with the most stringent security requirements.
- Spartan-6 FPGAs support Device DNA and AES. The AES 256-bit configuration protection is the same in Virtex-5 FPGAs and Spartan-6 FPGAs. AES will protect the configurations bit stream. Once a valid bit stream is loaded, a Device DNA scheme can be applied by the designer.

11. Will the AES key be hard coded (Efuses) or battery backed up like the Virtex-4 and Virtex-5 FPGAs ?

- In Spartan-6 FPGAs, the AES protection is only on the two largest devices (LX100 and LX150). It will be implemented similar to Virtex-5 FPGAs. Virtex-6 FPGAs will provide both battery back up and EFuse key storage.

12. Why has the logic architecture changed from Virtex-5 FPGA family to Virtex-6 FPGA family?

- Xilinx realized that the usability of the LUT-6 architecture could be enhanced for some applications with the simple addition of an extra flip flop. Heavily pipelined designs, as well as DSP-intensive designs (relying on a lot of smaller LUTs), will benefit greatly from this improvement. Given that the silicon impact is minimal, Xilinx decided to add the flip-flop to the CLB architecture.

13. Why did you remove the LX platform in the Virtex-6 FPGA family?

- When looking at our entire customer base and the evolution of their systems, we realize that an overwhelming majority of designs targeting Virtex-6 devices will use transceivers. In addition, the removal of transceivers would not allow for an increase in other features (due to packaging restrictions, etc.).
- To this end, the Virtex-6 LXT and SXT platforms offer devices with both transceivers and a large number of SelectIO™ pins. Customers that do not need the transceivers

Virtex-6 and Spartan-6 FPGA Families -- Frequently Asked Questions

can disable them and use the device without using the transceivers. They will still get the rich mix of IO, BRAM, and logic that would have been expected with an LX platform device.

14. Are there going to be any performance improvements for the MicroBlaze™ processor in the Virtex-6 FPGA family?

- The MicroBlaze soft core processor running on a Virtex-6 device should see the same 15% performance improvement expected for similar speed grades in the fabric vs. the Virtex-5 FPGA. The extra flip-flop for every LUT is estimated to give the MicroBlaze processor additional performance improvement.

15. Does the Virtex-6 memory controller solution for DDR3 memory support DIMMs?

- Yes. The DDR3 memory controller will support DIMMs, including the required leveling behavior.

16. Can designs be ported from previous generations to the new families?

- Yes. Both the Virtex-6 and Spartan-6 Families allow migration of designs from previous generation Virtex and Spartan devices.

SERIAL IO TECHNOLOGY

17. What are the capabilities of the GTX, GTP, and GTH transceivers?

- Virtex-6 FPGA GTX transceivers are based on the same architecture as the proven Virtex-5 FPGA GTX transceiver with improvements and additions in key areas. GTX transceivers cover data rates from 150Mbps to 6.5Gbps, and are designed to meet stringent CEI-6 jitter specifications with focus on performance and ease of use. The transceiver has been optimized for superior signal integrity with the integration of Decision Feedback Equalizer (DFE), in addition to linear EQ and Tx pre-emphasis. The GTX transceiver offers tremendous flexibility in clocking that enables independent data rates between the Tx and Rx. With the integration of 64b/66b and 64b/67b gearbox, GTX simplifies high line-rate designs saving thousands of logic cells in the design implementation.
- Spartan-6 FPGA GTP transceiver is also based on the proven Virtex-5 FPGA GTX architecture in the low cost 45nm process technology with focus on cost and ease of use. The GTP transceiver covers key protocol standards between 614Mbps and 3.2Gbps. The GTP transceiver is designed with circuits for Rx linear equalization and Tx pre-emphasis as well as built-in support for out-of-band signaling schemes required in PCI Express and SATA.
- Virtex-6 FPGA GTH transceivers cover data rates up to 11.4Gbps and are designed to address the growing high bandwidth requirements in the 40G and 100G systems.

18. What are the differences between the Virtex-6 FPGA GTX transceiver, the Spartan-6 GTP transceiver, and the Virtex-5 FPGA GTX transceiver?

Virtex-6 and Spartan-6 FPGA Families -- Frequently Asked Questions

- The Virtex-6 GTX transceiver is based on the Virtex-5 FPGA family GTX transceiver and shares most of its building blocks. It has greater flexibility when it comes to supporting a wide set of different standards on a single device. Given that the Virtex-6 FPGA GTX transceiver is based on the production-qualified Virtex-5 FPGA GTX transceiver, Xilinx has an extremely high level of confidence in the GTX technology.
- The Spartan-6 FPGA GTP transceiver addresses the low cost market with support up to 3.2Gbps line rates while the GTX supports up to 6.5Gbps. The Spartan-6 FPGA process technology emphasizes cost and hence has different transistor characteristics. Key applications targeted for the GTP include PCIe, displays and communications. (Please see the protocols supported in Question 20.)
- Competing devices only offer a limited number of full feature transceivers (32 in the EP4S530GX) and the rest are 3.25Gbps PMA-only links. The PCS layer for these channels has to be implemented in the fabric which can run into several thousand logic cells. All the transceivers in the Virtex-6 FPGA LXT platform are identical, meaning that they all can run up to 6.5Gbps and have PMA and PCS (including 8b/10b, 64b/66b and 64b/67b encoding), built-in channel bonding, and decision feedback equalization.

19. What is the lower operating rate of the Virtex-6 FPGA GTX transceivers?

- The Virtex-6 FPGA GTX transceivers will support line rates as low as 150Mbps.

20. What high-speed serial protocols are supported?

- Virtex-6 FPGA GTX transceiver supports all the key protocols in the range of 150 Mbps – 6.5Gbps. The most notable ones are Gigabit Ethernet, PCI Express Gen1 & Gen2, XAUI, Serial Rapid IO, CPRI, OBSAI, HD-SDI, OC-48, OTU1, and CEI-6 among others.
- Spartan-6 FPGA GTP transceiver supports key protocols up to 3.125Gbps. The most notable ones are Gigabit Ethernet, PCI Express Gen1, XAUI, Displayport, CPRI, and OBSAI among others.

21. What support does the Virtex-6 PCIe block offer?

- The Virtex-6 PCIe hard block macro will support PCIe Gen1 and Gen2 interfaces with line rates of 2.5Gbps and 5Gbps, respectively. This hard macro will support endpoint operations as well as downstream port operations. Each block will be able to support up to 8 lanes (for Gen1) and up to 4 lanes (for Gen2).

22. What is the plan for 8x Gen2 and future PCIe interface support for Virtex-6 products?

- The Virtex-6 FPGA base platform will not support Gen2 x8 interface as a hard macro. However, Northwest Logic has a soft IP solution for a PCIe Gen2 x8 interface for the Virtex-5 FPGA FXT platform which will be ported to the Virtex-6 platform as well.

Virtex-6 and Spartan-6 FPGA Families -- Frequently Asked Questions

- The Virtex-6 FPGA base platform will not support PCIe Gen3 interface, neither as a hard macro nor as a complete PHY with the GTH transceiver for two reasons. First, the PCIe Gen3 specifications is not yet finalized, so anyone claiming Gen3 support today is taking a bet on where the standards will end up. Secondly, PCIe adoption shows that Gen3 will not start shipping in the Virtex-6 delivery time frame.
- The Virtex-6 FPGA GTH transceiver will actually be able to support the 8Gbps rate. However, the GTH transceiver will not be fully compliant to the PCIe v3.0 electrical specification such as out-of-band signaling and ground referenced receiver. In a very limited number of applications (such as test equipment manufacturers who are early adopters), this may be a reasonable solution.

VIRTEX-6 FPGA FAMILY

23. Will Virtex-6 FPGAs support partial reconfiguration?

- Yes, Xilinx plans to support partial reconfiguration with Virtex-6 FPGA platforms.

24. Why isn't there a PowerPC processor optimized for Virtex-6 devices?

- As we review market requirements for next-generation embedded processing systems, we realize that the capabilities necessary to meet these requirements will not be possible using our current system. We are exploring technical options that will allow us to best serve the embedded marketplace. In the meantime, our Virtex-5 FXT FPGA platform provides the capabilities required by our customers developing embedded systems from now until our next generation product solution is available.

25. Why is the Virtex-6 FPGA not pin-to-pin compatible with the Virtex-5 FPGA?

- With each generation of our Virtex product families, we target the most optimal IO placement on the die and reduce crosstalk between IOs for each of the packages. However, in order to maintain backward pin compatibility, performance could potentially be compromised. Therefore, Xilinx decided not to offer pin-to-pin compatibility between the Virtex-5 FPGA and Virtex-6 FPGA families in order to provide the highest performance with the highest signal integrity possible for Virtex-6 devices.
- In addition, the Virtex-6 IO architecture has dramatically changed (split IO columns in the center with full regional and IO clock support). These architectural changes make pin-compatibility with previous architectures virtually impossible without adversely impacting Virtex-6 FPGA performance.

FOUNDRY PARTNERSHIPS

26. Why Does Xilinx use multiple foundries?

- Xilinx maintains a flexible manufacturing strategy to support business continuity and provide the best cost structure. To this end, we don't restrict ourselves to a single

Virtex-6 and Spartan-6 FPGA Families -- Frequently Asked Questions

foundry when evaluating the technology and partnerships that best suit the fulfillment of our customers' needs.

27. Why Was Samsung added as a foundry partner?

- While Xilinx does not disclose the specifics of Xilinx manufacturing operations, it is important to note that Samsung brings a rich set of capabilities to FPGA users: Samsung is aligned with Xilinx's strategy to optimize for power, performance, and cost and is recognized by the industry as a proven manufacturer with a well-established, low power, and advanced process technology. Samsung is also a Common Platform™ supplier along with IBM and Chartered Semiconductor providing additional leverage through industry-wide collaboration.

28. What's the status of your relationship with UMC?

- Our successful partnership with UMC for more than a decade over more than 12 process nodes continues with next-generation Xilinx FPGAs. In particular, our tremendous success at the 65nm node is the latest example of this most productive relationship. As pioneers across multiple process generations, such as the first use of triple-oxide technology in an FPGA, UMC and Xilinx maintain their commitment to work together in delivering the world's leading FPGAs optimized for power, performance and cost.

29. What will be your relationship with Toshiba going forward?

- Toshiba is a valued partner with whom we have a very successful fabrication partnership. Toshiba will continue to manufacture production wafers for Xilinx.

ECOSYSTEM SUPPORT

30. Is there software support available for the new FPGA families?

- Yes. Beta software has been provided to early access customers today, enabling them to begin working with Virtex-6 and Spartan-6 FPGA Families. General availability of software supporting both Virtex-6 and Spartan-6 FPGA Families is targeted for the second calendar quarter of 2009.

31. What boards will be available for embedded processing and high-speed serial IO development?

- We will release domain-specific boards that extend the capabilities provided by the base boards using Virtex-6 and Spartan-6 FPGAs. These domain-specific boards will include extendable FMC daughter boards that address DSP, embedded processing, and connectivity.

32. Given the change in logic structure, will the Synplify and Precision synthesis tools support the additional flip-flop right away?

- Yes. This does not depend on Synthesis tools but on ISE for place and route.