Section 11

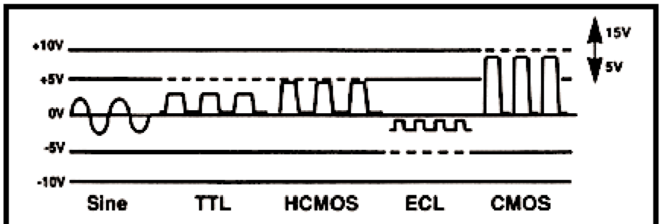
Application Notes

VECTRON

1. Clock Oscillators and Non-Compensated Sinewave Crystal Oscillators

For the moderate stability crystal controlled oscillator where neither temperature compensation nor oven operation are required, there are three primary parameters: output wave shape, frequency and accuracy/stability.

A. Output. The vast majority of systems require a crystal oscillator output which is TTL compatible, ECL compatible, CMOS compatible or sinusoidal. Any of these outputs can be simply generated by circuits which follow the crystal oscillator stage. These are illustrated in Figure 1 with a dashed line in each case representing supply voltage input and the solid line showing the output.

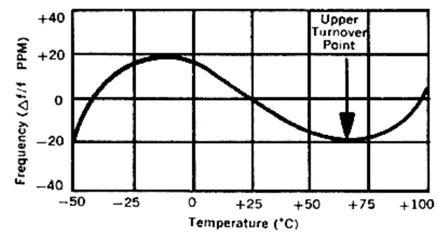


– Figure 1 –

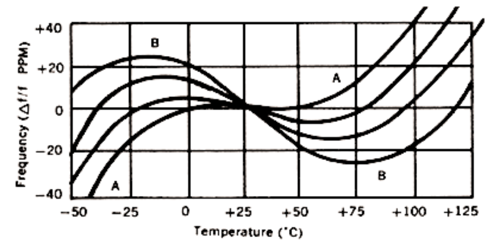
B. Accuracy/Stability. The most basic element in an oscillator specification is the output frequency. At any given time however, the oscillator's output frequency will differ from the desired specified frequency resulting in a frequency error. This error is comprised of three primary components:

1. Initial accuracy. This is generally defined as the difference between the oscillator output frequency and the specified frequency at 25°C at the time of shipment by the oscillator manufacturer. When specifying accuracy it is assumed that the user has no provisions to adjust the oscillator's output frequency. When a frequency tuning control is included, accuracy no longer needs to be specified; instead the range and settability of the tuning adjustment become more consequential.

2. Temperature Stability. Figure 2 shows a typical characteristic of crystal frequency vs. temperature. It is one of a family of curves illustrated in Figure 3. Figure 3 shows that one extreme, curve A, has a relatively flat slope (good temperature stability) near room temperature, but is very frequency sensitive at high and low temperatures. The other extreme, curve B, shows greater sensitivity near room ambient but also provides the overall best temperature stability over wide temperature ranges. The angle at which the quartz crystal is cut determines the temperature characteristic of a specific crystal. The proper characteristic from this family of curves is select, for each individual crystal oscillator requirement In a well designed oscillator the stability vs. temperature is determined primarily by the temperature characteristic of the crystal, and the oscillator manufacturer must select the crystal characteristics which conform with the oscillator circuit to insure that the intrinsic stability of the crystal is not degraded.



—Figure 2—



—Figure 3—

A temperature stability of, for example, ± 10 ppm over 0°C to +50°C means a peak-to-peak frequency change of 20 ppm over the specified temperature range, not referenced to the frequency at any specific temperature. This is the generally accepted definition of temperature stability which, in MIL-0-5531 0, is called "frequency-temperature stability".

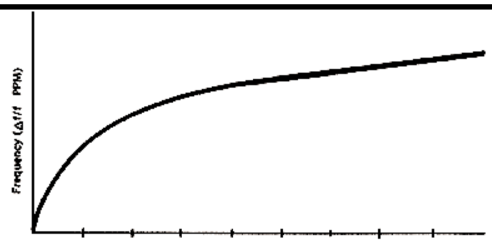
Clock & Sinewave Oscillators

If a reference temperature is desired with a maximum allowable frequency change from that reference, it should be specified, for example, as "±10 ppm over O°C to +50°C referenced to the frequency at +25°C."

While Vectron segregates initial accuracy and temperature stability, the two may be combined in specifying an overall allowable error for oscillators with no frequency tuning adjustment. The appropriate term is "frequency-temperature accuracy" and it is the maximum allowable deviation from the specified nominal frequency over a given temperature range.

1. Clock Oscillators and Non-Compensated Sinewave Crystal Oscillators

3. Aging (Long-term stability). Aging refers to the continuous change in crystal operating frequency with time, all other parameters (temperature, supply voltage, etc.) held constant. The better the processing of the crystal, the lower the aging rate (that is, the higher the long-term stability). Figure 4 shows a typical aging curve. It illustrates that when a crystal oscillator is initially turned on by the manufacturer, the crystal ages rapidly but its stability improves with time. While the aging rate will typically continue to improve with time, most crystals achieve close to their lowest aging rate within several months after turn-on. As long as crystal current is moderate, solder sealed or resistance welded AT-cut crystals used in most clock oscillators provide typical aging of 5 ppm during the first year and 3 ppm per year thereafter (5 ppm = .0005% = $5x10^{-6}$). If the error introduced by this degree of crystal aging exceeds that allowed in the user's system, this can be overcome by



—Figure 4—

(1) specifying the inclusion of a frequency tuning adjustment in the oscillator to permit periodic recalibration and/or, (2) using a higher quality crystal. Improved aging to 1 x 10^{-6} per year can be achieved by employing a specially processed crystal housed in an evacuated glass or coldweld sealed holder. Because aging generally introduces a small part of the overall error in moderate stability clock oscillators, it is often ignored in specifying these devices.

There are numerous other factors contributing to crystal oscillator instability, such as affect of supply voltage variation, load variation and physical orientation; however, they are not significant with respect to the major errors already detailed and are therefore excluded from discussion in this clock oscillator section.
In summary, for most clock oscillator requirements, a specification will be sufficiently complete if it includes the following electrical elements: frequency, output level (wave shape), supply voltage, initial accuracy and temperature stability.

Following are examples of specifications for clock oscillators illustrating the considerations described in this discussion.

Vectron Model	CO-402A-OX	XO-400-DFC-C	CO233T-3
Output	10.24 MHz	155.52 MHz	122.560 MHz
Output Level	TTL Compatible (drives 10 loads)	PECL Complementary	sinewave,0.5 vrms minimum into 50 ohms
Input Voltage	5Vdc ±5%	3.3 Vdc ±5%	15 Vdc ±5%
Accuracy	±.005%	Included in 10 year aging in temp. stability budget	Tuning adjust settable to ±.0001%
Temp Stability	0°C to +70°C ±.0025%	0°C to +70°C ±.0020%	0°C to +50 °C ±0.0003%
Size	0.5” x0.8” x.20”	0.5” x0.8” x.22”	1.5”x1.5”x0.625”
Mounting:	14 pin DIP Compatible	14 pin DIP Compatible	Printed circuit board pins

Note that the CO-233T-3 which provides a high degree of temperature stability (± 0.0003%) includes a tuning adjustment to permit accurate settability. While occasionally a need arises for high temperature stability concurrent with a loose initial accuracy tolerance, generally stability and accuracy go hand in hand for a "balanced" specification. Similarly, it is generally illogical to include a tuning adjustment for precise settabililty when the stability requirements are very loose.

When the overall accuracy/stability specification becomes too stringent to be met with a simple clock oscillator, improvements can be accomplished in three areas:

1. The initial accuracy error may be essentially eliminated and aging periodically compensated for by incorporating into the oscillator a frequency adjustment as previously discussed.

2. Aging may be improved by using a higher grade crystal, as previously discussed, and with a higher grade circuit maintaining low constant crystal current.

3. The temperature stability may be improved by using temperature compensation techniques or housing the oscillator in an oven.

2. VCXO's Voltage Controlled Crystal Oscillators VCO's Voltage Controlled Oscillators. Non-Crystals

A VCXO (voltage controlled crystal oscillator) is a crystal oscillator which includes a varactor diode and associated circuitry allowing the frequency to be changed by application of a voltage across that diode. This can be accomplished in a simple clock or sinewave crystal oscillator, a TCXO (resulting in a TC/VCXO-temperature compensated voltage controlled crystal oscillator), or an oven controlled type (resulting in an OC/VCXO-oven controlled voltage crystal oscillator).

There are several characteristics peculiar to VCXOs. In generating a VCXO specification these apply in addition to the characteristics which define fixed frequency crystal oscillators. Primary among the specifications which are peculiar to VCXOs are the following:

Control Voltage - This is the varying voltage which is applied to the VCXO input terminal causing a change in frequency. It is sometimes referred to as Modulation Voltage, especially if the input is an AC signal.

Deviation - This is the amount of frequency change which results from changes in control voltage. For example. a 5 volt control voltage might result in a deviation of 100 ppm, or a 0 to + 5 volt control voltage might result in total deviation of 150 ppm.

Transfer function (sometimes referred to as Slope Polarity) - This denotes the direction of frequency change vs control voltage. A positive transfer function denotes an increase in frequency for an increasing positive control voltage, as in Figure 1 A. Conversely, if the frequency decreases with a more positive (or less negative) control voltage, as in Figure 1 B, the transfer function is negative.

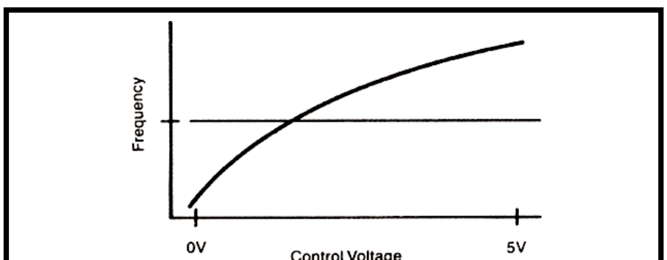


Figure 1A

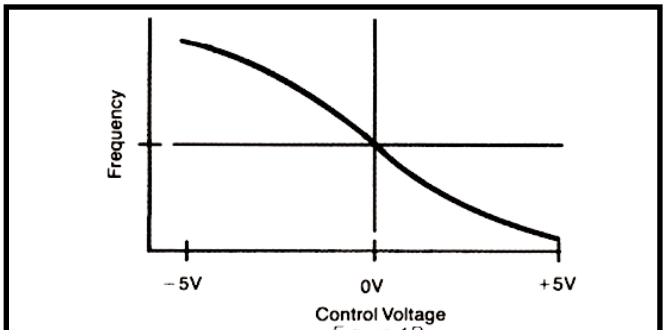


Figure 1B

Linearity - The generally accepted definition of linearity is that specified in MIL-PRF-55310. It is the ratio between frequency error and total deviation, expressed in percent, where frequency error is the maximum frequency excursion from the best straight line drawn through a plot of output frequency vs control voltage. If the specification for an oscillator requires a linearity of ±5% and the actual deviation is 20 kHz total as shown in Figure 2, the curve of output frequency vs control voltage input could vary ± 1 kHz (20 kHz ±5%) from the Best Straight Line "A". These limits are shown by lines "B" and "C". "D" represents the typical curve of a VCXO exhibiting a linearity within ±5%.
In Figure 3, the maximum deviation from Best Straight Line "A" is - 14 ppm and the total deviation is 100 ppm, so the linearity is ±14ppm/100 ppm = ±14%.

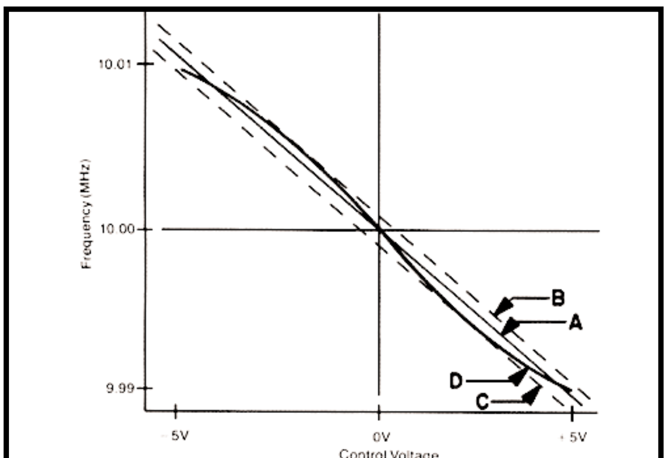


Figure 2

Figure 2

2. VCXO's Voltage Controlled Crystal Oscillators VCO's Voltage Controlled Oscillators. Non-Crystals

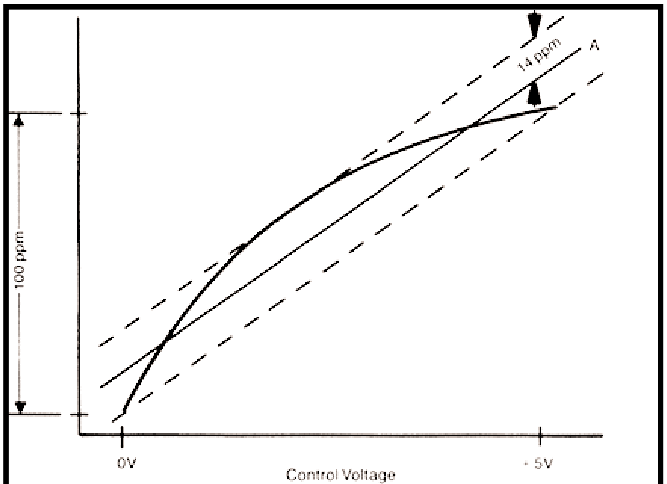


Figure 3

The VCXO which produces the characteristic indicated in Figure 2 uses a hyper-abrupt junction varactor diode, biased to accommodate a bipolar (±) control voltage. The VCXO which produces the characteristic in Figure 3 uses an abrupt junction varactor diode with an applied unipolar control voltage (positive in this case).

Good VCXO design dictates that the voltage to frequency curve be smooth (no discontinuities) and monotonic. All Vectron VCXOs exhibit these characteristics.

Modulation rate (sometimes referred to as Deviation Rate or Frequency Response) - This is the rate at which the control voltage can change resulting in a corresponding frequency change. It is measured by applying a sinewave signal with a peak value equal to the specified control voltage, demodulating the VCXO's output signal, and comparing the output level of the demodulated signal at different modulation rates. The modulation rate is defined by Vectron as the maximum modulation frequency which produces a demodulated signal within 3 dB of that which is present with a 100 Hz modulating signal. While non-crystal controlled VCOs can be modulated at very high rates (greater than 1 MHz for output frequencies greater than 10 MHz), the modulation rate of VCXOs is restricted by the physical characteristics of the crystal. While the VCXO's modulation input network can be broadened to produce a 3 dB response above 100 kHz, the demodulated signal may exhibit amplitude variations of 5-15 dB at modulation frequencies greater than 20 kHz due to the crystal.

Slope/Slope Linearity/Incremental Sensitivity - This can be a confusing area as these terms are often misapplied. Slope should be really called average slope if it is intended to define the total deviation divided by the total control voltage swing. For the VCXO depicted in Figure 2, the average slope is -20 kHz * 10 volts = -2 kHz/volt. Incremental sensitivity, often misnomerred Slope Linearity means the incremental change in the frequency vs control voltage. Thus, while the average slope in this example is -2 kHz per volt, the slope for any segment of the curve may be considerably different from -2 kHz/volt. In fact, for VCXOs with Best Straight Line linearity of ±1% to ±5%, the Incremental Sensitivity is approximately (very approximately) 10 times as great as the Best Straight Line linearity. Thus a VCXO with ±5% Best Straight Line linearity can exhibit a slope change of ±50% on a per volt basis. Therefore, a specification which reads "Slope: 2 kHz/volt ± 10%" requires clarification as it could mean either Average Slope or Incremental Sensitivity. If it were intended to define average slope, it simply specifies a total deviation of 18 kHz to 22 kHz and would more properly have stated, "Total Deviation: 20 kHz - 10%." However, if it were intended that the frequency change for each incremental volt must fall between 1.8 kHz and 2.2 kHz, a highly linear VCXO is being specified as a ±10% Incremental Sensitivity relates approximately to a ±1% Best Straight Line linearity. That element of the specification should read, "Incremental Sensitivity: 2 kHz ± 10% per volt."

Other Design Considerations

Stability - A quartz crystal is a high Q device which is the crystal oscillator's stability determining element. It inherently resists being "pulled" (deviated) from its designed frequency. In order to produce a VCXO with significant deviation, the oscillator circuit must be "de-Q'd". This results in degrading the inherent stability of the crystal in terms of its frequency vs. temperature characteristic, its aging characteristic, and its short-term stability (and associated phase noise) characteristic. Therefore, it is in the user's best interest not to specify a wider deviation than that absolutely required.

2. VCXO's Voltage Controlled Crystal Oscillators VCO's Voltage Controlled Oscillators. Non-Crystals

Phase Locking - When a VCXO is used in phase lock loop application, the deviation should always be at least as great as the combined instability of the VCXO itself and the reference or signal onto which it is being locked. Vectron produces a line of VCXOs especially intended for use in phase lock loop applications (described on the pages which follow). However, if the open loop stability requirements of a system are more stringent than available in this product line, a TC/VCXO may be required. For the highest stability open loop requirements, the appropriate oscillators may be those described in the TCXO or OCXO sections of this catalog, incorporating a narrow deviation VCXO option, rather than those described in the VCXO section.

Basic Oscillator Frequencies - Fundamental mode crystals (generally 10-25 MHz) permit the widest deviation, while 3rd overtone crystals (generally 20-70 MHz) allow deviation approximately 1/9th of that which applies to fundamentals. Therefore, all wide deviation VCXOs (greater than ±100 to ±200 ppm deviation) use fundamental crystals; narrower deviation VCXOs can use fundamental mode or 3rd overtone crystals, the selection of which often depends upon such specifications as linearity and stability. It is rare that higher overtone, and therefore higher frequency crystals find application in VCXOs. Thus, VCXOs with output frequencies higher or lower than available from the appropriate crystal frequencies include frequency multipliers or dividers.

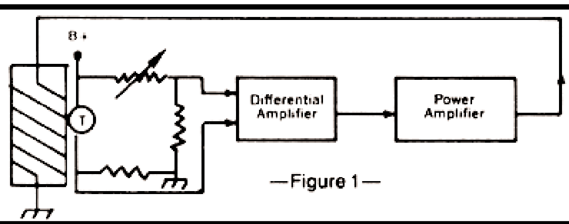
General Note - While it is true of any type of crystal oscillator, it is especially important with VCXOs that the user not over-specify the product. The particular problem with VCXOs is that increased deviation results in degraded stability which can result in the need for still wider deviation, further degrading stability, resulting in a spiraling increase in the required deviation.

3. OCXO's Oven Controlled Crystal Oscillators

If stability requirements are too stringent to be met by a basic crystal oscillator or TCXO, the crystal and critical circuits may be temperature controlled by an oven. The block diagram for a Vectron oven controlled crystal oscillator is similar to that for a Vectron TCXO except that the varactor diode and associated thermistor compensation network are deleted and the oscillator is instead temperature controlled by a proportionally controlled oven.

Proportional Oven Controlled

A proportional control is an electronic servo system which continuously supplies power to the oven; it varies the amount of oven power, continuously compensating for the ambient temperature changes. In many Vectron oven controlled oscillators, a thermistor is heat sunk to the oven's metal shell to sense temperature. The thermistor is one leg of a resistance bridge, as shown in the following diagram.



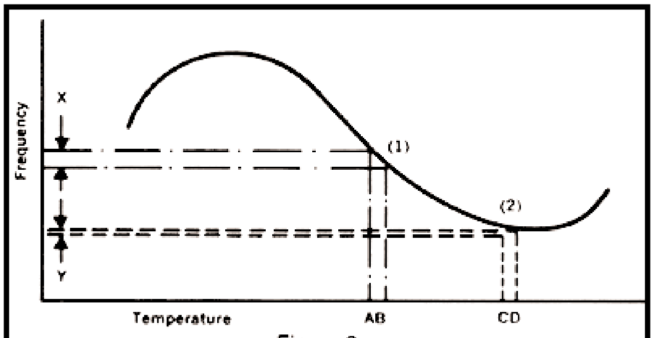
—Figure 1—

The bridge operates such that if the temperature at the oven decreases due to an ambient temperature change, the change in thermistor resistance causes the bridge to unbalance, developing an increase in bridge output voltage. This voltage is amplified in a high-gain differential amplifier. The output of the differential amplifier is further amplified in a power amplifier which drives directly into the oven winding. Thus, the small voltage increase resulting from bridge unbalance generates a large voltage increase across the oven winding. This increase in power to the oven generates more heat, compensating for the temperature decrease which was initially sensed by the thermistor. Similarly, an increase in temperature at the oven causes a reduction in bridge output voltage, which results in reduced power into the oven and a compensating temperature decrease.

An alternative to this design, used in some Vectron oven shell as the heat transfer mechanism, in lieu of having a heater winding. The concept is the same, the only difference being the vehicle by which the heat is applied to the oven.

Employing a proportionally controlled oven can improve oscillator temperature stability relative to the crystal's inherent stability by more than 5000 times (from ±1x10-5 to ±1x10-9 over 0-50°C, for example). However, the oven control system is not perfect because (a) the open loop gain is not infinite, (b) there are internal temperature gradients within the oven and (c) circuitry outside the oven which is subjected to ambient temperature changes can "pull" the frequency. Therefore, a change in ambient temperature will result in small changes in oven temperature.

Setting Oven Temperature



—Figure 2—

As shown above, the actual temperature to which the oven is set is critical in minimizing the effect of ambient temperature change.

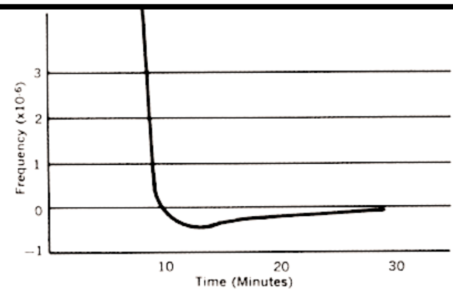
Referring to Figure 2, if the oven temperature were set to the point designated as (1), and a change in ambient temperature caused a change in oven temperature from A to B, a frequency change of magnitude X would result. However, if the oven temperature were set to the upper turnover point (2), an equal temperature change (C to D) would result in a significantly reduced change in frequency (magnitude Y). Therefore, each Vectron oven is individually set to the turnover temperature of the crystal which it houses. This is accomplished by adjusting the potentiometer shown as one leg of the bridge in Figure 1.

Warmup with AT cut crystals

When an oscillator is initially turned on at room temperature the frequency is extremely high relative to the output frequency after the oven stabilizes, typically by $30x10^{-6}$. This is simply due to the fact that the frequency of an AT cut crystal is considerably higher at room temperature than at its upper turnover temperature. As the perature than at its upper turnover temperature. As the oven warms up, the crystal frequency rapidly decreases. In standard Vectron oscillators, the oven balances in 10^{-15} minutes but the crystal displays a rubberband effect and overshoots its final frequency per Figure 3, prior to stabilizing. Typically, relatively high degree of stability is achieved within 30 minutes after turn-on; this time can be reduced to less than 5 minutes in special fast warm-up designs.

Turnover Temperature

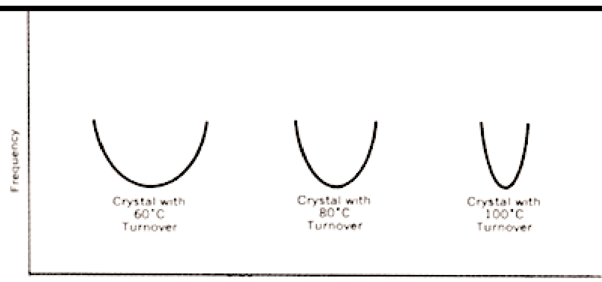
The oven operating temperature (crystal turnover temperature) must be several degrees higher than the highest ambient temperature in which the oscillator is to operate in order that the oven may maintain good control (considering the internal heat rise generated by the oscillator itself).



—Figure 3—

However, there are disadvantages associated with high oven temperature operation. First, the crystal's frequency vs. temperature characteristic is sharper with higher turnover crystals resulting in more sensitivity to minute changes in oven temperature as shown in Figure 4.

Second, and more important, crystal aging (discussed below) degrades with an increasing temperature. Therefore, in designing an oven controlled crystal oscillator, one is faced with a compromise in determining the desired oven operating temperature; it should be low as practicable, but it must be high enough to provide good control at the maximum ambient operating temperature.



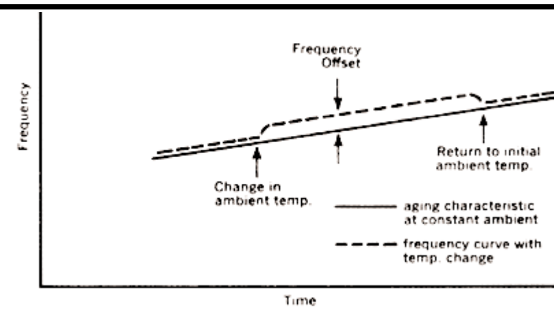
—Figure 4—

Stability

A. Aging - Aging refers to the continuous change in crystal oscillator frequency with time, all other parameters held constant. Prior to delivery, each Vectron oven controlled oscillator is pre-aged until it achieve its specified aging rate. Aging rate is often used synonymously with the word stability; thus, an oscillator with an aging rate of one part in 10^{-8} per day ($1x10^{-8}$/day) is sometimes referred to as one part in 108 oscillator. This is incorrect terminology, as aging rate (long term stability) must be referred to time, and represents only one facet of oscillator stability.

B. Temperature Stability - As previously noted, because no oven control system is perfect, a change in ambient temperature causes a small change output frequency. The frequency shift is an offset from the oscillator's aging curve. This deviation from the normal aging characteristic is not related to time, but is a fixed offset. Thus, the frequency offset vs. temperature (temperature stability), for a given temperature change is, for example, $5x10^{-9}$, not $5x10^{-9}$/day. This characteristic is shown below.

Ambient temperature changes do not produce hysteresis effects; that is, if there is a change in ambient temperature followed by a return to the original temperature, the final frequency will be essentially that which would have resulted had there been no ambient temperature change.



—Figure 5—

When the required temperature stability is beyond that which can be achieved with a standard proportionally controlled oven, a double oven system can be employed in which the standard oven is housed within a second oven. The outer oven then buffers the ambient temperature changes to the inner oven, which contain the oscillator circuit.

3. OCXO's Oven Controlled Crystal Oscillators

C. Restabilization And Retrace - When a crystal oscillator is turned off for a period of time and then turned on again (as occurs when the unit is shipped), the crystal requires a restabilization period. The characteristic is similar to the initial factory aging characteristic, but high stability is achieved significantly more quickly because the crystal has been factory pre-aged.

In most applications, oven-controlled crystal oscillators are continuously energized. This being the case, aging is the critical characteristic with turn-off/turn-on characteristic being of little or no significance. However, certain applications require that oven controlled crystal oscillators be frequently de-energized and re-energized (a practice which should be avoided whenever possible). When applications require frequent turn-off, an additional series of characteristics should be considered.

In Figure 6, assume that an oscillator is energized until time T2 when it is turned off for a period of time and then turned on again at time T3. Three characteristics may then be of significance:

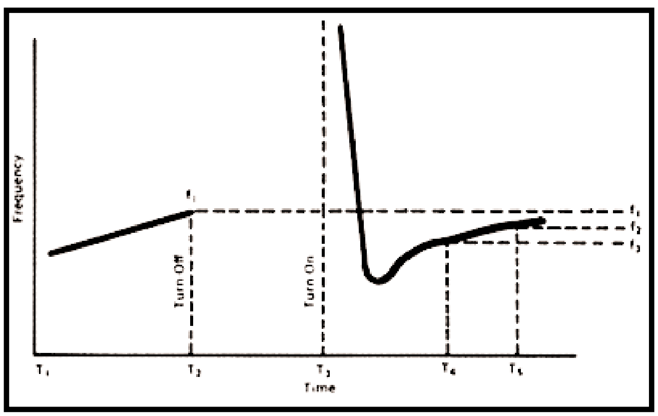


Figure 6

1. How close does the oscillator return to the output frequency at turn-off, a specified time after turnon. This is called the retrace characteristic. Retrace error at $T_4 = f_1 - f_3$.
2. How much will the frequency change over moderate periods of time (hours) after the oven has stabilized. This is called the restabilization, or warmup, characteristic. Restabilization rate from T_4 to $T_5 = (f_3 - f_2) / (T_5 - T_4)$
3. How long does it take the oscillator to achieve its specified aging rate following a specified off period (This is called "reaging").

Many factors affect retrace, restabilization and reaging characteristics. Proper circuit design and component selection minimize their effects, leaving (1) the crystal and, (2) the length of off-period prior to oscillator turn-on as the prime factors. There is significant variation in these characteristics from crystal to crystal and they should only be specified when absolutely required and then only to the degree needed, as "tight" specifications in this area can have a major impact upon oscillator cost due to low yield. These characteristics are of little consequence in oscillators which are energized continuously.

Double Rotated (SC and IT Cut) Crystals

While most high stability crystal oscillators use AT Cut Crystals, SC and IT Cut Crystals are often used in the highest stability models.

An SC Cut Crystal is one of a family of double rotated crystals (quartz crystals cut on an angle relative to two of the three crystallographic axes). Others in the family include the IT Cut and FC Cut. The SC Cut represents the optimum double rotated design as its particular angle provides maximum stress compensation, but similar performance is achieved with the IT Cut.

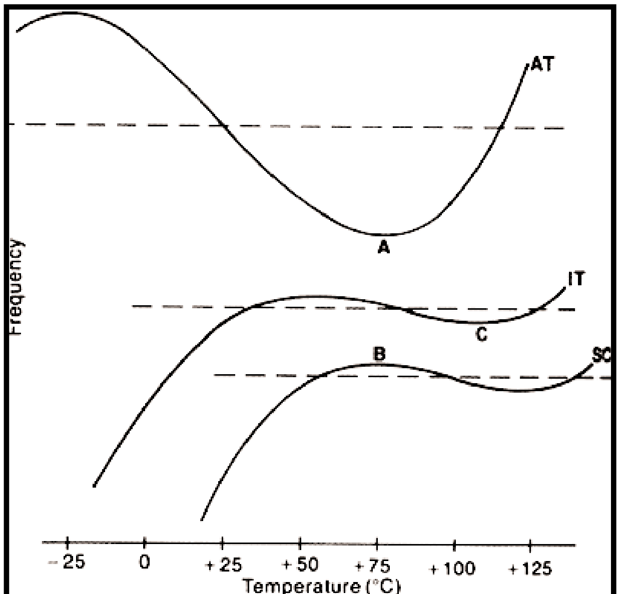
Following is a comparison between double rotated (referred to simply as SC for convenience) and AT Cut crystals.

Advantage of SC Crystals:

1. *Improved Aging*. For a given frequency and overtone (e.g. 10 MHz, third overtone), the SC crystal provides 2:1 to 3:1 aging improvement relative to AT crystals.
2. *Warm-up.* In oven controlled oscillators with a given oven design and turn-on power, the SC crystal achieves its "final frequency" in considerably less time than does the AT crystal.
3. Phase Noise. For a given oscillator design, crystal frequency and overtone, the SC crystal provides higher Q and associated improved phase noise characteristics. This improvement applies primarily close to the carrier as the noise floor is determined by circuit design rather than the crystal.
4. *High Operating Ambient Temperature*. Figure 7 shows the relative frequency-temperature characteristics of AT, IT and SC crystals. The upper tem-

3. OCXO's Oven Controlled Crystal Oscillators

perature turnover point of the AT crystal ("A" in Figure 7) and lower temperature turnover point of the SC crystal ("B" in Figure 7) are optimally in the 70°C to 90°C temperature range. Based upon (a) the desired 1O°C difference between the highest operating ambient temperature and the crystal



—Figure 7—

turnover temperature, and
(b) the manufacturing tolerance of crystal turnover temperatures, these crystals are best suited for maximum operating ambient temperatures of 50°C to 75°C. However, the upper temperature turnover point of the IT crystal ("C" in Figure 7) is well suited to higher temperature operation and thus the IT crystal is a logical choice for high stability oven controlled oscillators having a maximum operating temperature in the 85°C to 95°C range. Note that while SC and IT crystal curves are relatively flat at elevated temperatures, their frequency falls off rapidly at low temperatures. Thus, while they serve well in high stability HIF oven controlled oscillators, they are generally not well suited for other types of stable crystal oscillators.

5. *Orientation Sensitivity (tip-over)*. When the physical orientation of an oscillator is changed, there is a small frequency change (typically not more than several parts in 10^{-9} for any 90 degree rotation), due to the change in stress on the crystal blank resulting from the gravitational affect upon the crystal supports. Tip-over is expressed in 10^{-9}/g where one g represents one half of a 180° orientation change. The SC crystal is less frequency sensitive to orientation change than is the AT. However, the tip-over difference between AT and SC crystals is not consequential for most applications and this characteristic is usually not a specification consideration.

6. *Spurious Under Vibration.* When a crystal oscillator is subjected to vibration, spurious frequencies are generated, offset from the frequency oscillation by the frequency of vibration. The amplitude of these spurious outputs is related to the amplitude of vibration, the mechanical design of the crystal support, and the mechanical design of the oscillator. The SC crystal produces lower amplitude spurious output under vibration than does the AT; however, this characteristic is determined more by the mechanical designs of the crystal and oscillator than by crystal cut.

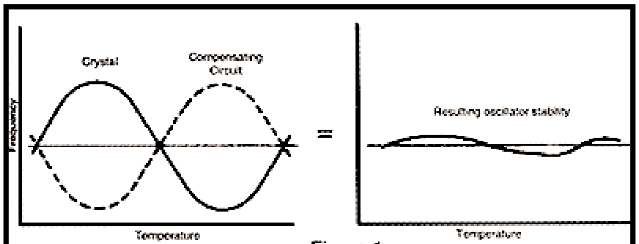
Disadvantages of SC Crystals:

1. *Cost*. Because of difficulties associated with tightly-controlled angle rotations around two axes in the manufacture of SC crystals vs one axis for the AT, the SC crystal is significantly higher in cost than that of an AT of the same frequency and overtone.
2. *Pullability*. The motional capacitance of an SC crystal is several times less than that of an AT of the same frequency and overtone, thus reducing the ability to "pull" the crystal frequency. This restricts the SC crystal from being used in conventional TCXOs and VCXOs, or even in oven controlled oscillators requiring the ability to deviate the frequency of oscillation by any significant degree.

In summary, the suitability of double rotated crystals for use in crystal oscillators is essentially restricted to those oven controlled applications where the improved aging, warm-up, and close-in phase noise characteristics justify a significant cost increase.

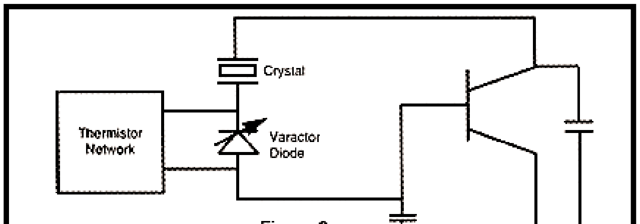
4. TCXO's Temperature Compensated Crystal Oscillators

A. Temperature Stability. The temperature stability of a basic crystal oscillator can be improved by incorporating in the oscillator circuit components with temperature characteristics approximately equal to and opposite



—Figure 1—

from that of the crystal as shown in Figure 1.
The actual technique employed in all except the most



—Figure 2—

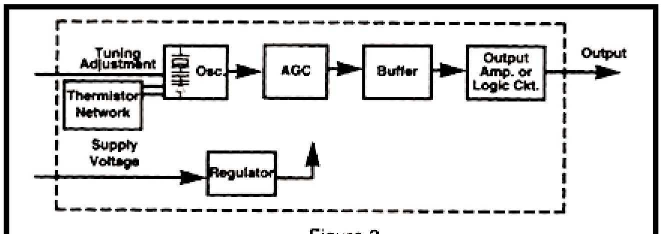
simple TCXOs is based upon use of a varactor diode in series with the crystal as follows:
A change in voltage "V" causes a change in the capacitance of the varactor diode resulting in a change in frequency of oscillation. The thermistor network is tailored to the crystal to cause voltage "V" to vary with temperature in a manner which will compensate for the crystal's frequency versus temperature characteristic. As each individual TCXO requires that its compensation network be matched to its individual crystal, the cost of a TCXO is closely related to the difficulty of the frequency versus temperature specification. The stability requirements of most TCXOs dictate compensation by means of a multiple thermistor network with several interdependent variable components thus making the solution of simultaneous equations by computer the only practical approach to temperature compensation.

When an oscillator manufacturer specifies a stability of $\pm 1 \times 10^{-6}$ over -20°C to of + 70°C, this means a total peak error of 2×10^{-6} over the temperature range, not referenced to the frequency at any specific temperature. If a reference, such as room temperature, is desired with a maximum allowable error of $\pm 1 \times 10^{-6}$ from that reference, the specification should clearly state $\pm 1 \mathrm{X} 10^{-6}$ over -20°C to +70°C referenced to the frequency at +25°C." Further, it should be noted that the frequency versus temperature characteristic of a TCXO is not linear; thus a $2 \mathrm{xl} 0^{-7}$ total error over O°C to +50°C will not produce a gradient of $2 \times 10^{-7} \div 50 = 4 \times 10^{-9}$ per ºC. Perturbations in the crystal characteristics (activity dips) make it virtually impossible to guarantee exceptional stability on a per degree basis in TCXOs.

B. Aging. In clock oscillators with moderate temperature stability, aging is usually of little consequence. However, in highly temperature stable TCXOs, crystal aging becomes a significant factor in the oscillator's overall frequency error. Therefore, TCXOs employ specially processed crystals in evacuated glass or coldweld holders.*

Many TCXO specifications include both moderate and long term aging requirements such as $\pm \mathrm{lxlO}^{-6}$ per year. The latter actually has more rapaning for a TCXO because the temperature sensitivity of the device makes it almost impossible to measure $\pm 1 \times 10^{-8}$ per day aging except under constant environmental conditions; the small day to day changes in even laboratory ambient temperatures will cause greater frequency shifts than those resulting from crystal aging over short time periods.

C. Other Factors: Figure 3 illustrates the block diagram for a typical Vectron TCXO.



– Figure 3 –

App Notes

4. TCXO's Temperature Compensated Crystal Oscillators

It shows those elements generally not required in simple clock oscillators, but included in the proper design of a highly stable TCXO: (1) a frequency compensation network to minimize temperature sensitivity, (2) a precision crystal coupled with AGC for minimum aging, (3) a multiturn tuning adjustment permitting precise setting of frequency, (4) buffering following the oscillator to minimize the effects of external circuit changes and (5) an internal regulator to minimize the effects of voltage variation. Each of these elements is a factor in properly specified TCXO, an example of which follows.

Vectron Type:	TC-210-DAB-307A
Frequency:	12.8 MHz
Output Level:	HCMOS
Supply Voltage:	3.3 Vdc ±5%
Current Drain:	<15 mA
Temperature Stability:	±3 x 10^{-7} over 0°C to +50°C
Supply Variation:	±1 x 10^{-8} percent change in supply
Aging:	3.5 x 10^{-6} per 10 years
Electrical Frequency Adjustment:	±5 ppm minimum via external voltage, 0 to Vdd.

5. Phase Noise

Signal sources such as crystal oscillators produce a small fraction of undesirable energy (phase noise) near the output frequency. As performance of such systems as communications and radar advance, the spectral purity of the crystal oscillators which they employ is increasingly critical.

Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1 Hz bandwidth at a given offset from the desired signal. A plot of responses at various offsets from the desired signal is usually comprised of three distinct slopes corresponding to three primary noise generating mechanisms in the oscillator, as shown in Figure 1. Noise relatively close to the carrier (Region A) is called Flicker FM noise; its magnitude is determined primarily by the quality of the crystal. Vectron's best close-in noise results have been obtained using 5th overtone AT cut crystals or 3rd overtone SC cut crystals in the the 4-6 MHz range. While not quite as good on average, excellent close-in noise performance may also be achieved using 3rd overtone crystals in the 10 MHz area, especially double rotated types (see page 41 for a discussion of double rotated SC and IT cut crystals). Higher frequency crystals result in higher close-in noise

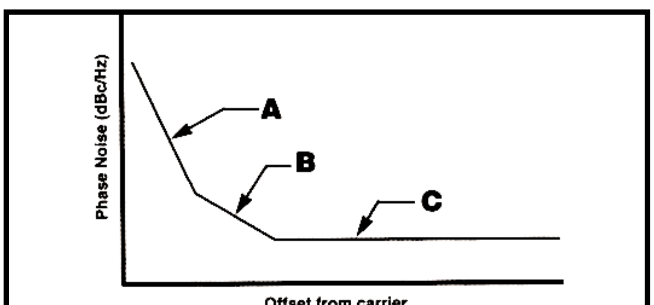


Figure 1

because of their lower Q and wider bandwidths.
Noise in Region B of Figure 1, called "1/F" noise, is caused by semiconductor activity. Design techniques employed in Vectron low noise "L2" crystal oscillators limit this to a very low, often insignificant, value.

Region C of Figure 1 is called white noise or broadband noise. Special low noise circuits in Vectron "L2" crystal oscillators offer dramatic improvements (15-20 dB) relative to standard designs.

When frequency multiplication is employed to achieve the required output frequency from a lower frequency crystal, the phase noise of the output signal increases by 20 log (multiplication factor). This results in noise degradation of approximately 6 dB across the board for frequency doubling, 10 dB for frequency tripling and 20

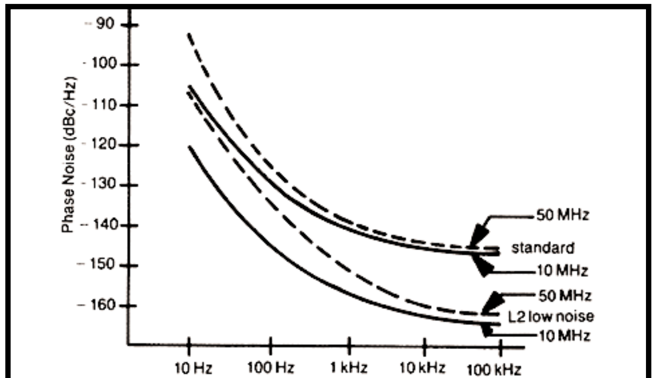


Figure 2

dB for decade
multiplication. As shown in Figure 2, the noise floor is almost independent of the crystal frequency for oscillators which do not employ frequency multiplication. Thus for low noise floor applications, the highest frequency crystal which satisfies long-term stability requirements should generally be used. However, when a higher frequency application specifically requires minimum close-in phase noise, lower frequency crystals may often be multiplied to advantage. This is so because close-in phase noise is disproportionately better than the noise performance obtained using higher frequency crystals.

Note that the introduction of a varactor diode and moderate Q crystal, used typically in TCXO and VCXO products, result in poorer close-in noise performance when compared with fixed frequency non-compensated crystal oscillators.

Phase Noise Testing

The phase noise test characterizes the output spectral purity of an oscillator by determining the ratio of desired energy being delivered by the oscillator at the specified output frequency to the amount of undesired energy being delivered at neighboring frequencies. This ratio is usually expressed as a series of power measurements performed at various offset frequencies from the carrier, the power measurements are normalized to a 1 Hz bandwidth basis and expressed with respect to the carrier power level.

5. Phase Noise

This is the standard measure of phase fluctuations described in NIST Technical Note 1337 and is called (f). Figure 3 shows a block diagram of the method suggested by NIST, and used by Vectron, to measure (f). Signals from two oscillators at the same nominal fre-

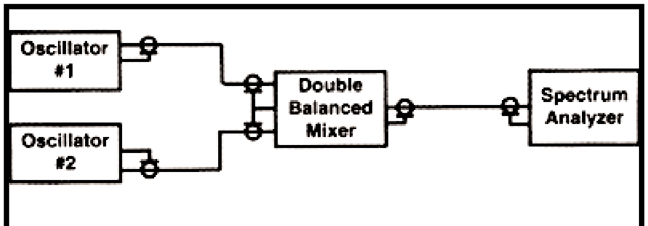


Figure 3—General Block Diagram

quency are applied to the mixer inputs. Unless the oscillators have exceptional stability, one oscillator must have electronic tuning for phase locking. A very narrow band phase-locked loop (PLL) is used to maintain a 90 degree phase difference between these two sources. The mixer operation is such that when the input signals are 90 degrees out of phase (in quadrature), the output of the mixer is a small fluctuating voltage proportional to the phase difference between the two oscillators. By examining the spectrum of this error signal on the spectrum analyzer, the phase noise performance of this pair of oscillators may be measured. If the noise of one oscillator dominates, its phase noise is measured directly. A useful and practical approximation when the two test oscillators are electrically similar is that each oscillator contributes one-half the measured noise power. When three or more oscillators are available for test, the phase noise of each oscillator may be accurately calculated by solving simultaneous equations expressing data measured from the permutations of oscillator pairs.

Figure 4 shows a practical system of measurement Of (f). The steps taken to measure phase noise with this system are:

1. Calibration of the spectrum analyzer screen.
2. Phase lock the oscillators and establish quadrature.
3. Record spectrum analyzer readings and normalize readings to dBc/Hz SSB per oscillator. These steps

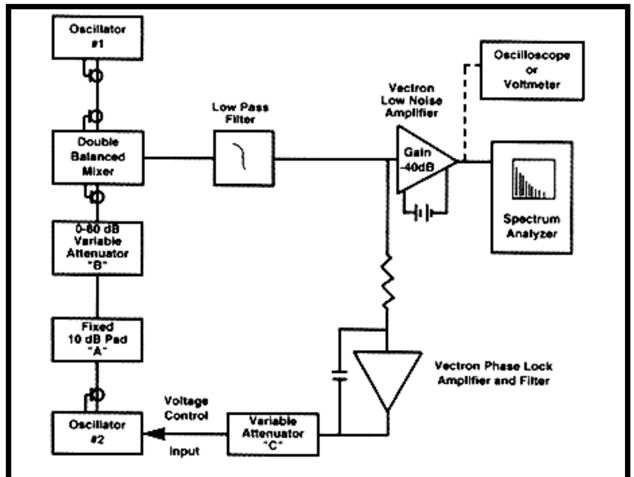


Figure 4 – Measurement System

are detailed below.

Step I - Calibration

To avoid saturating the mixer, the signal level of one oscillator is permanently attenuated by 10 dB pad (Attenuator "A"). During the calibration, the level of this oscillator is additionally attenuated by 80 dB (Attenuator "B") to improve the dynamic range of the spectrum analyzer. The oscillators are mechanically offset in frequency and the amplitude of the resulting low frequency beat signal represents a level of -80 dB; it is the reference for all subsequent measurements. When using a swept spectrum analyzer, this level is adjusted to the top line of the spectrum analyzer's screen. When using a digital (FFT) spectrum analyzer, the instrument is calibrated to read RMS VOLTS/ relative to this level . When full level is restored to the mixer, and the oscillators are phase locked, the phase noise will be measured with respect to this -80 dB level.

5. Phase Noise

Step II - Phase Lock

The oscillators are phase locked to quadrature by mechanically adjusting them to the same frequency. The desired 90 degree phase difference between the two oscillators is indicated when the mixer output is 0 Vdc. An oscilloscope or zero-center voltmeter connected temporarily at the input to the spectrum analyzer is a convenient way to monitor progress toward quadrature. The operating bandwidth of the PLL must be much lower than the lowest offset frequency of interest because the PLL partially suppresses phase noise in its bandwidth. A widely used empirical method of establishing an appropriate loop bandwidth is to progressively attenuate the voltage control feedback via Attenuator "C". By comparing successive noise measurements at the lowest offset frequency of interest while advancing Attenuator "C", an operating point may be found where the measured phase noise is unaffected by changes in the attenuator setting. At this point the loop bandwidth is not a factor of the measured phase noise.

Step III - Readings

Readings are taken with respect to the -8OdB calibration level previously established in Step 1. Smoothing or averaging is used if the spectrum analyzer is so equipped to avoid measurement variations. Swept spectrum analyzer readings generally require each of the following corrections while digital analyzer readings displayed in RMS/ do not require the first two corrections. The analyzer's manual should be consulted regarding corrections for analyzer noise response.

	Correction
1. Normalize to 1 Hz bandwidth. "BW" is the measurement bandwidth. Calculation assumes the noise is flat within the measurement bandwidth.	**10 log (1/BW)**
2. Video response of swept analyzer to noise signals.	**+3 dB**
3. Double sideband to single sideband display.	**-6 dB**
4. Contribution of two oscillators assuming they are of equal noise quality.	**-3 dB**

6. Jitter in Clock Sources

Continuous advances in high-speed communication and measurement systems require higher levels of performance from system clocks and references. Performance acceptable in the past may not be sufficient to support high-speed synchronous equipment. Perhaps the most important and least understood measure of clock performance is jitter.

The purpose of this discussion is fourfold.
1. To define jitter intuitively, and discuss it's properties.
2. To explain how jitter degrades system performance.
3. To describe various practical methods of measuring jitter, including the relevance and ease of each method.
4. Offer guidelines for specifying high-speed clocks and related devices.

Jitter Defined:
Jitter: "Short-term variations of the significant instants of a digital signal from their ideal positions in time" (ITU).
The expected edges in a digital datastream never occur exactly where desired. Defining and measuring the timing accuracy of those edges (jitter) is critical to the performance of synchronous communication systems.

Digital Waveform with Jittered Edges

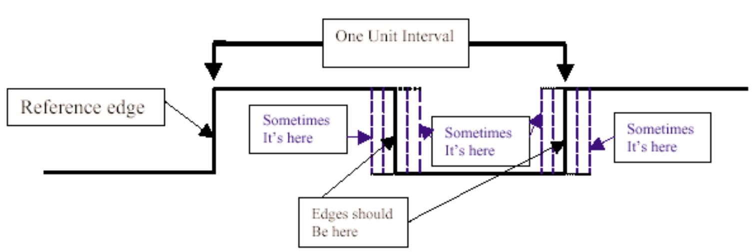


Figure 1

Definition of terms:
a) Jitter expressed in Unit Intervals: A single unit interval is one cycle of the clock frequency. This is the normalized clock period. Jitter expressed in Unit Intervals describes the magnitude of the jitter as a decimal fraction of one unit interval.
b) Jitter expressed in degrees (deg.): Jitter expressed in degrees describes the magnitude of the jitter in units of deg. where one cycle equals 360 deg.
c) Jitter expressed in absolute time: Jitter expressed in units of time describes the magnitude of the jitter in appropriate orders of magnitude, usually picoseconds.
d) Jitter expressed as a power measurement is described in units of radians or unit intervals squared. Often expressed in dB relative to one cycle-squared (From Bellamy) [1]
e) Pattern Jitter: Pattern dependent jitter. Sometimes referred to as flanging. Not random in nature. Generally a result of subharmonics. When viewed in the time domain, it is seen as multiple modes of jitter. Pattern jitter is deterministic, it is a phenomenon that may be attributed to a unique source. All other jitter referred to in this discussion is stochastic in nature, and may only be described as a random variable with respect to time.

For example:
Assume a clock rate of 155.52 MHz. One unit interval would be equal to the period of the signal, 1/155.52 MHz = 6.43 nsec. = 360 deg.
Assume 100 ps Pk-Pk of jitter.
100 Ps of jitter = .01555 unit intervals (UI) of jitter = 5.598 deg. of jitter. (All Pk-Pk) All three measurements describe the same amount of jitter.

For jitter power, rms (one sigma, s) measurements are used. For the above case, we approximate Pk-Pk as 7s, or 7 times the RMS value, placing the rms. jitter power at .0000049 UI 2 . {(.01555/7) 2 . Expressed in dB, relative to one unit interval, jitter power in this case would be 10log (.0000049)= -53.1 dBui. As will be seen later, jitter can be derived from power spectral density (phase noise) measurements. Table 1 relates various measures of jitter in a 155.52 MHz system clock

Pk-PkJitter in Seconds	Degrees	Unit interval	Unit Interval	Jitter Power
6.43E-09 = one cycle	Degrees(Pk-Pk) *normalized*	Pk-Pk UNITS *normalized*	RMS UNITS *normalized*	dBui
1.00E-10	5.60	0.015552	0.0022217	-53.07
2.00E-11	1.12	0.003110	0.0004443	-67.05
			(1/7 of Pk-Pk approximation)	

Table 1

6. Jitter in Clock Sources

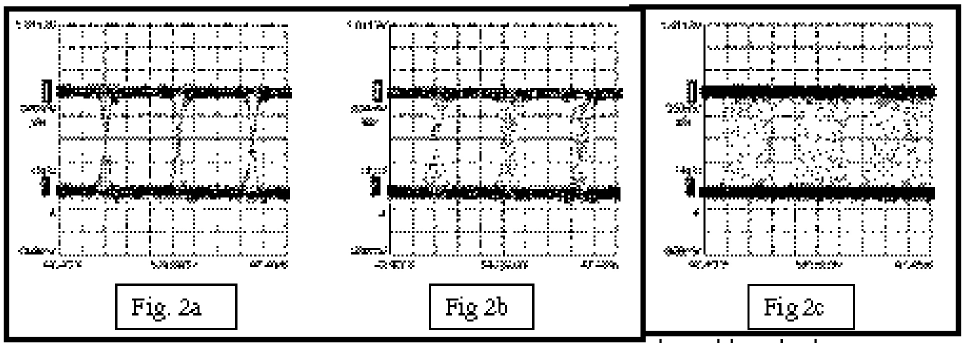


Fig. 2a Fig 2b Fig 2c

Jitter Bandwidth and Spectral Content

The displacement of edges in Fig.1 is a result of noise. Noise has spectral content as well as power. Consequently, the edge jitter in Fig.1 also has spectral content. The edges in Figure 1 vary randomly with time, however the noise that causes the jitter is not necessarily uniform over all frequencies. Jitter due to 10 kHz noise could be greater or less than jitter due to 100 kHz noise. Spectral content of clock jitter differs greatly depending on the technique used to generate the clock. Measured jitter also varies with measurement technique and jitter bandwidth. Improperly specified or measured jitter might result in unnecessary costs, or poor system performance. See references [2,3] for additional information on defining and specifying jitter in telecom systems. Jitter characteristics of various clock sources is discussed later in this article.

How Does Jitter Effect System Performance

The effects of jitter on communication systems are well beyond the scope of this discussion. Refer to references [1,4] for a more thorough treatment. A simple discussion may help to understand the deleterious effects of jitter in digital systems. Every bit of data transmitted over synchronous communication systems is sampled for its value at the receiver. The sampled data can only have the value of logical one or zero. The optimum point for sampling data is at the center of each transmit clock cycle. In order to perform this function, the receiver aligns its own clock with the clock used to transmit the data. Figs.2, a, b, and c represent ideal, typical, and corrupted datastreams respectively. Commonly referred to as an "eye diagram" each graph is a cumulative graphical portrait of the edge placement due to noise or jitter. Ideally, sampling occurs at the center of the "eye". As edge jitter increases, the apparent eye begins to close. As a result, the likelihood of an error, i.e..... mistaking a logical one for a zero is more likely. Jitter due to oscillator noise is only one source of jitter in a telecom system. System designers must consider many sources of noise in telecom systems. The jitter introduced by clock sources is one component of noise, and becomes only one part of an "error budget" that must be weighed against performance requirements and cost.

Measurement Techniques

Time Domain Measurements
Edge to Edge Jitter Using a Delay Line

A true measure of clock jitter is the accurate position of clock edges over time. The most direct method of examining the placement of edges would be to look at the edges using an oscilloscope. Unfortunately, using standard oscilloscope techniques it is impossible to identify individual clock edges in absolute time. Any jitter measured with a standard oscilloscope is due to trigger instability. As a result, direct waveform measurements using an oscilloscope (even a very good oscilloscope) are not valid measurements of jitter. An additional technique is used to locate the reference edge, discriminate with time, and examine the jitter on following edges. Figure 3 illustrates this method with a

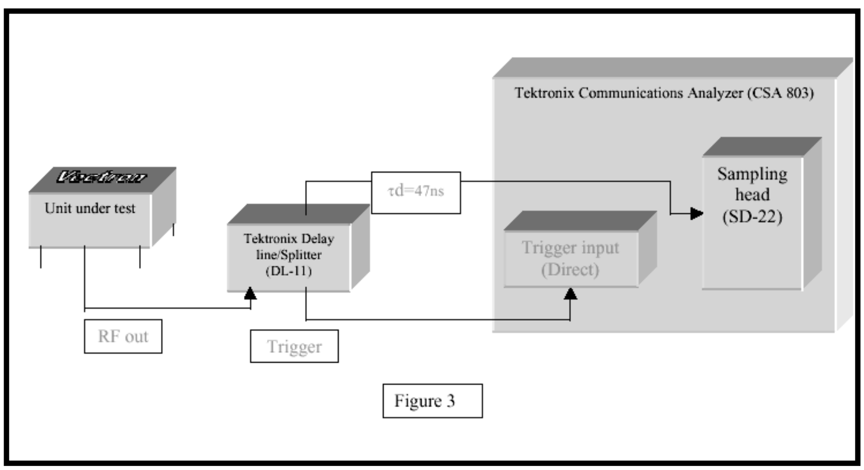


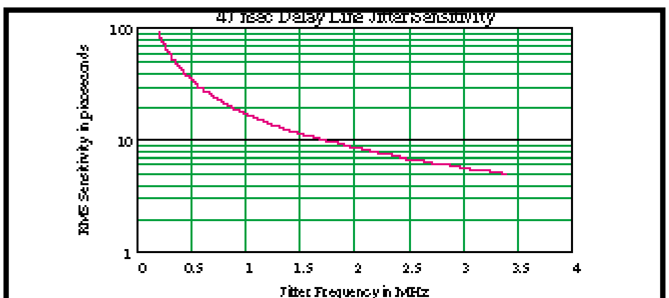
Figure 3

App Notes

6. Jitter in Clock Sources

typical configuration.
The output of the unit under test is fed into splitter /delay line. The non-delayed output o the splitter is fed to the external trigger input of the oscilloscope (a CSA-803 in this case). The delayed output of the DL-11 is connected to the input of the oscilloscope. By examining the clockstream at a time after the trigger equal to the delay used (in this case, 47 nsec), the trigger-edge is located. After the triggered edge has been identified, the next edge is examined. A histogram plot is then produced of the measured jitter of the second edge.

A CSA-803 is used for its statistical and histogram capabilities. This is a useful technique limited by the length of the delay line and the speed/sensitivity of the oscilloscope. For all frequencies greater than 1/(2ptd), the measurement is limited by the noise of the oscilloscope. Below 1/(2ptd), the sensitivity drops approximately 20 RMS Sensitivity in picoseconds dB/decade. For the 47-nsec delay shown in fig 3, the corner frequency occurs at 3.3 MHz. All jitter due to frequencies above 3.3 MHz



Sens(f)=1/2*π*τd*f*r
Where:
Sens(f) = jitter sensitivity
τd = amount of delay used
f = the jitter frequency to be measured
r = oscilloscope resolution

can be resolved to approximately 5 ps using the CSA-803. Jitter at 330 kHz can not be resolved below 50 ps. In a similar manner, jitter at 33 kHz can not be measured below 500 ps. Figure 4 is a plot of RMS jitter sensitivity using a 47-nsec delay line. It is critical to understand the advantages and limitations of this measurement method. For the numerical example given, low frequency jitter below 300 kHz would not be seen. Conversely, jitter due to sidebands 3.0 MHz offset or more could easily be identified. This test method is appropriate when measuring oscillators that employ

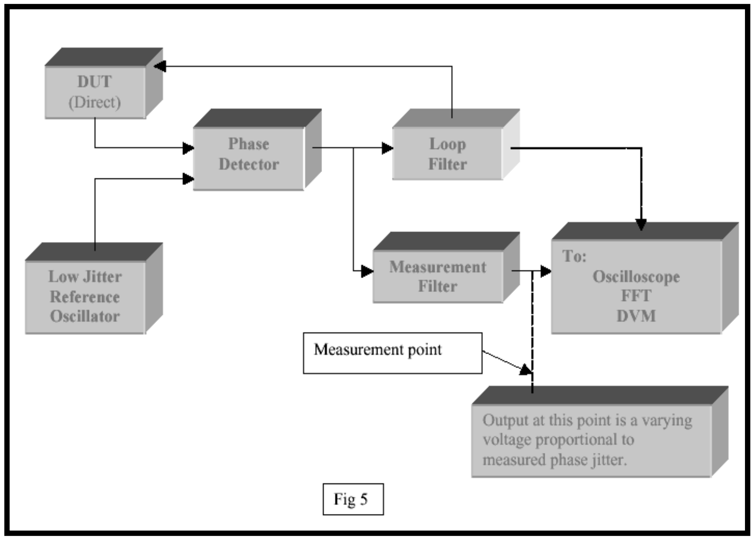


Fig 5

direct frequency multiplication or where low frequency jitter is not considered. (See previous description of Pattern Jitter).

Jitter Measurements Using Phase Locked Loops

It was noted that the length of the delay line limits resolution when measuring edge jitter. In order to measure jitter below 100 Hz offset, one needs merely to order up about three hundred miles of very low loss

delay line. In lieu of such a device, phase locked loops are used for a variety of noise measurements.
Figure 4 shows the basic elements of a phase locked loop (PLL) used to measure the noise of a clock source. Gardner [5], Best [6], and Woolover [7] are three excellent references for understanding PLLs. Some key loop requirements follow:

- The PLL loop bandwidth is a critical parameter for successful measurements. The system will only measure jitter frequencies outside (higher than) the loop bandwidth. It is recommended that the loop bandwidth be set to a maximum of 1/10 the lowest jitter frequency of interest.
- Loop damping must be set to at least 5 in order to reduce jitter peaking in the PLL. Jitter peaking will increase measured jitter.
- The measurement filter corresponds to jitter bandwidths recommended in Bellcore and ITU specifications. Refer to [2,3] for a list of jitter bandwidths and specifications. Band limiting needs to be defined as a pre-condition for any valid measurement.

6. Jitter in Clock Sources

· The output of the phase detector (PD) is a varying DC signal that is proportional to the varying phase due to jitter. It is necessary to know the gain constant (Kd) of the PD in volts/radian in order to quantify the detected jitter. For example, a phase detector with a Kd equal to 1 millivolt per degree will have a peak to peak output of 10 mV for an oscillator with 10 deg,. pk-pk jitter. It may be necessary to inject a known amount of jitter in order to calibrate the system for accurate measurements.

Jitter Measurements Using Phase Locked Loops: Interpreting the Data.

· In The Time Domain The output signal of the phase detector in Figure 5 contains a wealth of information about the jitter of the measured clock. Direct examination of the signal using an oscilloscope can show Pk-Pk jitter. A true RMS voltmeter can be used to measure RMS (one sigma) jitter. For these measurements, it is critical that the measurement filters used represent the band of jitter frequencies of interest. It would make no sense to measure noise from dc to 10 MHz when a bandwidth of 10 kHz to 1 MHz is required. Oscilloscopes with histogram and statistical capabilities are useful for characterizing the measured jitter.

In the Frequency Domain, the spectrum of the output signal from the phase detector in Figure 4 represents the spectrum and relative amplitude of jitter in the frequency domain. Examining the spectrum with a low frequency or FFT analyzer gives the most intuitive picture of clock jitter in terms of spectrum. By integrating the signal jitter spectrum over the frequency of interest, it is possible to derive the RMS jitter of the clock. This is the most accurate and unfortunately the most cumbersome method for characterizing jitter, requiring specialized test equipment. A numerical example is included in appendix I.

Specifying Jitter Performance

Good jitter performance and low cost are not mutually exclusive as long as:

· The system requirements for jitter are defined in terms of amplitude and spectrum.

· The method used to generate the clock output frequency is optimal for the application.

Application Performance Requirements

System Application	Degree of difficulty	Low Frequency Jitter Importance	High Frequency Jitter Importance	Possible Type see table 2
Radar	Very difficult Noise Application	Critical	Critical	A,B,C,D
Ultrasound/MRI	Very difficult Noise Application	Critical	Critical	A,B,C,D
Navigation/GPS	Difficult Noise Application	Critical	High	A,B,C,D
Transmission Systems (telecom)				
Public Network	Moderate Noise Application	Moderate	Moderate	A,B,C,D
Private Network (LAN)	Generally Easiest Application	Low	Low	A,B,F
Frequency Synthesis (see note 1)				
Low Freq. Reference		Moderate-Critical	Moderate-Low	A,B,C
High Frequency Source		Moderate-Low	Moderate-Critical	D,E,F

Note 1: Overall jitter performance is highly dependent on loop parameters.

Table 1

System Requirements:
Although it is impossible to address all possible variations, some general recommendations based on years of oscillator manufacturing may be helpful. While not a complete survey of all applications, Table 1 is a starting point for specifying oscillator performance. Jitter above 1 kHz is considered high frequency jitter.

Jitter Performance

Technique	Cost 1 is lowest 3 is highest	LF Jitter 1 is best 3 is worst	HF Jitter 1 is best 3 is worst	Comments	Type
Direct Clock/TCXO	1	2	1 or 2	Very Good Jitter	A
Direct VCXO	2	1	1 or 2	Very Good Jitter	B
Direct Oven	3	1	1	Excellent jitter	C
Tuned Multiplication	2	1	1 or 2	Periodic Jitter	D
Discrete PLL	2	2	2 or 3	Good Jitter	E
Monolithic PLL	1	3	2 or 3	Close in jitter is poor	F

Table 2

Clock Generation:

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6. Jitter in Clock Sources

Various methods may be employed to generate high frequency clocks. Performance may vary significantly based on the technique used. Below 20 MHz, it can be assumed that direct crystal frequency generation is sufficient for all but the most critical requirements. Low Noise options should be considered for low jitter applications for 20 MHz and above. Table 2 may be used as a starting point to select a cost-effective solution. Variations and combinations of methods listed in table 2 could also be optimal solutions.

CONCLUSION

To correctly specify performance of frequency sources both jitter frequency and amplitude should be considered. This requires an understanding of jitter, measurement techniques and their limitations. Time spent to determine system needs will result in fewer problems and less time spent fixing those problems later on. It will also determine a cost-effective approach for each application.

In this paper, we discussed the definition of jitter, the units used to describe it, and why jitter is an important parameter. We also reviewed techniques used to measure jitter as well as applications and typical performance based of various kinds of oscillators. The discussion is by no means complete, but should give the reader enough information to understand the issues involved. Industry standards were listed, as well as references for further reading. It is hoped that this paper is useful and considered a good starting point for understanding and specifying jitter.

7. rms Jitter Calculation

rms Jitter Calculation in the 12 kHz to 20 MHz Bandwidth for VI's VCO600A/VS500 @622.08 MHz

For applications requiring a 622.080, or 666.5143, MHz PECL/ECL VCO with the lowest possible jitter in the 50kHz to 80 MHz bandwidth, VI is offering the VCO600A/VS500 Series. These devices utilize SAW technology that resonates at a fundamental frequency eliminating the need for internal multiplication, which is usually required to achieve high frequencies. The net result is no harmonics/subharmonics and low phase noise, or in the time domain, low jitter. The phase noise was measured on several pairs of the VCO600A @ 622.080 MHz using an HP 3048A Phase Noise Measurement System. The typical phase noise was then integrated from 50 kHz to 80 MHz and converted to jitter using the methodology outlined in VI's "Jitter in Clock Sources" by Joe Adler, (available for download at VI's website www.vectron.com).

The following are the results:

X: = -54.95 dB Equivalent sideband level or the integrated phase noise

$J_{rms} := (360/(2p))\ 10^{\frac{X}{20}}$ = 0.1025 rms jitter in degrees

$J_{rms}/360$:= 0.0002847 Unit Intervals (UI) rms

$(J_{rms}/360)(1/622.080\text{MHz})$ = 0.458 ps rms or 3.206 ps peak to peak

The sideband level of -54.95 dBc for the integration of the phase noise over 50 kHz to 80 MHz has an equivalent jitter value of 0.458 ps RMS or 3.206 ps peak to peak.

rms Jitter Calculation in the 12 kHz to 20 MHz Bandwidth for VI's VCO600A/VS500 @622.08 MHz

For applications requiring a 622.080, or 666.5143, MHz PECL/ECL VCO with the lowest possible jitter in the 12kHz to 20 MHz bandwidth, VI is offering the VCO600A/VS500 Series. These devices utilize SAW technology that resonates at a fundamental frequency eliminating the need for internal multiplication, which is usually required to achieve high frequencies. The net result is no harmonics/subharmonics and low phase noise, or in the time domain, low jitter. The phase noise was measured on several pairs of the VCO600A @ 622.080 MHz using an HP 3048A Phase Noise Measurement System. The typical phase noise was then integrated from 12 kHz to 20 MHz and converted to jitter using the methodology outlined in VI's "Jitter in Clock Sources" by Joe Adler, (available for download at VI's website www.vectron.com).

The following are the results:

X: = -60.98 dB Equivalent sideband level or the integrated phase noise

$J_{rms} := (360/(2p))\ 10^{\frac{X}{20}}$ = 0.0051 rms jitter in degrees

$J_{rms}/360$:= 0.0014225 UI rms

$(J_{rms}/360)(1/622.080\text{MHz})$ = 0.230 ps rms or 1.610 pS peak to peak

The sideband level of -60.98 dBc for the integration of the phase noise over 12 kHz to 20 MHz has an equivalent RMS jitter value of 0.230 ps or 1.610 ps peak to peak.

rms Jitter Calculation in the 12 kHz to 20 MHz Bandwidth for VI's VC-400 Series VCXO

For applications requiring a PECL or ECL VCXO having an RMS jitter of < 1.0 ps within the bandwidth of 12KHz to 20 MHz, VI is offering our CO-400 Series. The phase noise on two VCXO's of VI's model VC-400-CFC-20SG @ 155.52 MHz were measured on the HP 3048A Phase Noise Measurement System. The phase noise was then integrated from 12 kHz to 20 MHz using the Trace Integration function of the 3048A. The equivalent sideband level of the integrated phase noise was -74.76 dBc. Per the methodology outlined in VI's "Jitter in Clock Sources" by Joe Adler, (available for download at VI's website www.vectron.com) the RMS jitter can be treated as small index phase modulation and can be converted from radians to degrees:

X:=-74.76 dB Equivalent sideband level or the integrated phase noise

$J_{rms} := (360/2\ )\ 10^{\frac{X}{20}}$ jitter in degrees.

$J_{rms}/360$ = 0.0000409 UI rms.

$(J_{rms}/360)$ (1/155.52 MHz) = 0.187 ps rms or 1.309 ps peak to peak.

The sideband level of -74.76 dBc for the integration of the phase noise over 12KHz to 20 MHz has an equivalent RMS jitter value of 0.187 ps. Therefore, the CO-600V series VCXO can satisfy the performance requirement of < 1ps RMS jitter for 12kHz to 20 MHz.

App Notes

7. rms Jitter Calculation

rms Jitter Calculation in the 12 kHz to 20 MHz Bandwidth for VI's J-Type Series VCXO

For applications requiring a PECL VCXO having an RMS jitter of <1.0 ps within the bandwidth of 12 kHz to 20 MHz, VI is offering our J type series. The phase noise on two VCXO's of VI's model JDUGLMEP-155.52 MHz were measured on the HP 3048A Phase Noise Measurement System. The phase noise was then integrated from 12 kHz to 20 MHz using the Trace Integration function of the 3048A. The equivalent sideband level of the integrated phase noise was -70./dBc. Per the methodology outline in VI's "Jitter in Clock Sources" by Joe Adler, (available for download at VI's website www.vectron.com) the RMS jitter can be treated as small index phase modulation and can be converted from radians to degrees:

X = -70.1 dB Equivalent sideband level or the integrated phase noise. (X)

Jrms = (360/2) 10 20 = 0.017911 degrees

Jrms/360 = 0.0000497 IT rms

(Jrms/360) (1/155.52 MHz) = 0.319 ps rms or 2.23

The sideband level of -70.1 dBc for the integration of the phase noise over 12 kHz to 20 MHz has an equivalent RMS jitter value of 0.319 ps. Therefore, the J Type series VCXO can satisfy the performance requirement of <1 ps RMS jitter for 12 kHz to 20 MHz.

rms Jitter Calculation in the 12 kHz to 20 MHz Bandwidth for VI's XO-500 Series XO

For applications requiring a PECL XO having an rms jitter of <1.0 ps within the bandwidth of 12 kHz to 20 MHz, VI is offering our XO-500 series. The phase noise on two VCXO's of VI's model XO-500 Series. The phase noise on two XO's of VI's model XO-500-DFC-20SN - 155.52 MHz were measured on the HP 3048A Phase Noise Measurement System. The phase noise was then integrated from 12 kHz to 20 MHz using the Trace Integration function of the 3048A. The equivalent sideband level of the integrated phase noise was -70.0 dBc. Per the methodology outlined in VI's "Jitter in Clock Sources" by Joe Adler, (available for download at VI's website www.vectron.com) the RMS jitter can be treated as small index phase modulation and can be converted from radians to degrees.

X = 70.0 dB Equivalent sideband level or the integrated phase noise (X)

Jrms = (360) (2) 10 20 = 0.0181185 degrees

Jrms/360 = 0.0000503 UI rms

(Jrms/360) (1/155.52 MHz) = 0.323 ps rms or 2.26 ps peak to peak

The sideband level of -70.0 dBc for the integration of the phase noise over 12 kHz to 20 MHz has an equivalent RMS jitter value of 0.165 ps. Therefore, the XO-500 series XO can satisfy the performance requirement of <1 ps RMS jitter for 12 kHz to 20 MHz.

rms Jitter Calculation in the 12 kHz to 20 MHz Bandwidth for VI's XO-400 Series XO

For applications requiring a PECL XO having an rms jitter of <1.0 ps within the bandwidth of 12 kHz to 20 MHz, VI is offering our XO-400 series. The phase noise on two XO's of VI's model XO-400 Series. The phase noise on two XO's of VI's model XO-400-DFC-20SN - 155.52 MHz were measured on the HP 3048A Phase Noise Measurement System. The phase noise was then integrated from 12 kHz to 20 MHz using the Trace Integration function of the 3048A. The equivalent sideband level of the integrated phase noise was -69.0 dBc. Per the methodology outlined in VI's "Jitter in Clock Sources" by Joe Adler, (available for download at VI's website www.vectron.com) the RMS jitter can be treated as small index phase modulation and can be converted from radians to degrees.

X = 69.0 dB Equivalent sideband level or the integrated phase noise (X)

Jrms = (360) (2) 10 20 = 0.020329 degrees

Jrms/360 = 0.0000564 UI rms

(Jrms/360) (1/155.52 MHz) = 0.363 ps rms or 2.54 ps peak to peak

The sideband level of -69.0 dBc for the integration of the phase noise over 12 kHz to 20 MHz has an equivalent RMS jitter value of 0.363 ps. Therefore, the XO-400 series XO can satisfy the performance requirement of <1 ps RMS jitter for 12 kHz to 20 MHz.

8. Absolute Pull Range Definition

Introduction

Vectron International uses Absolute Pull Range to define the amount of deviation a VCXO can be adjusted about the device's center frequency, (fo). This application note defines APR and compares the advantages with alternative terms such as total pull range.

Definition

APR is the minimum guaranteed amount the VCXO can be varied, about the center frequency (fo). It accounts for degradation's including temperature (0 to 70 or -40 to 85°C), aging (10 years, 40°C), power supply variations (10%) and load variations.

APR = (Pull range) - (degradations due to Temperature+aging+power supply+load)

For a VCXO specified in terms of APR, there is no guess work regarding how much frequency deviation is available, over all conditions, to track your incoming signal.

For example, one of the most popular APR options is 50 ppm, which is defined by "G" in the part number code. A 16.384 MHz VI V-Type VCXO would typically have no more than 20 ppm of temperature drift, 5 ppm of aging (10 years, 40C), 5 ppm due to power supply variation and 4 ppm due to load variations. A device specified in terms of Total Pull would need to have at least 84 ppm of Total Pull to
meet specifications.

In order to offer the APR guarantee, devices are well characterized for temperature, aging and power supply variations. Every VCXO is tested over temperature for pull range. This is a fully automated process where devices are continuously tested throughout a 0 to 70, or -40 to 85°C temperature cycle, including a soak at the extreme temperatures. Data is automatically stored for analysis. Aging characterization has been performed and correlated. Variations due to power supply and load are also well understood.

Devices specified with Total Pull Range can falsely seem superior due to what seems like a higher pull capability. However, in order to ensure that a VCXO specified in terms of Total Pull meets your design needs, the manufacturer must be contacted to define drifts due to temperature, aging, power supply and load variations, which must then be subtracted from their TPR. It can not be assumed that the VCXO performance is equal to Total Pull Range minus the "stability" unless the stability is clearly defined - this is seldom the case. APR reduces time spent defining and understanding VCXO specifications.

Example

In a digital communications network, the source clock has a defined maximum error from the center frequency over temperature, aging and power supply variations. This error is defined by a variety of factors dictated by the application. The receiver incorporates a VCXO which must be capable of tracking the source error to recover the clock and/or translate to a higher frequency. For example, a Stratum 4 level clock dictates a worse case error of 32 ppm over all environmental conditions. The VCXO must also be able to pull or track this 32 ppm over temperature, aging and power supply variations.

A VCXO specified in terms of APR with a 32 ppm APR would be the correct choice and will always be capable of locking to the source clock under the most adverse conditions - specmanship has been eliminated.

Again using a Stratum 4, definition the VCXO can be selected by;

VI's APR Method	**Other's TPR Method**
F= 32ppm APR	Total Pull Range
DONE !	minus temperature stability
	minus aging
	minus supply variations
	minus output load variations

Conclusion

APR is a superior method for specifying the deviation capability of a VCXO and is rapidly being adopted by other suppliers in the industry. In addition to testing to a minimum APR, every device is automatically tested for rise and fall time, duty cycle, current consumption and start-up time with test data stored for SPC analysis. As well as offering superior performance and packaging technology, VCXO's supplied by VI are the most thoroughly tested and have the best guaranteed specifications in the industry.

9. Saw-Based Frequency Control Product Applications

Introduction

In the first half of this paper, several SAW-based frequency control products which find applications in modern telecommunication systems like Synchronous Optical Network (SONET), Synchronous Digital Hierarchy (SDH), and Asynchronous Transfer Mode (ATM) will be presented. They play the important role of frequency synthesis, frequency translation, data and clock recovery, and clock signal distribution to ensure low bit error rate transport of signals in high frequency optical telecommunication equipment up to 2.5 Gb/s.

In the second half of this paper, the applications and the availability of low-loss RF and IF SAW filters for existing and emerging wireless systems, the competing technologies, the challenges to enter the market, and the applications of conventional high-loss and high-selectivity SAW filters in equipment based on the Code Division Multiple Access (CDMA) technique will be reviewed.

1.1 SAW-Based Timing Recovery Unit

The SAW-based timing recovery unit (TRU600) regenerates data and clock signals from corrupted NRZ digital data streams, such as those encountered in fiberoptic data link and telecommunication applications. Although there are many suppliers providing discrete SAW filters for timing recovery applications, the TRU600 allows an easy drop-in solution for users. SAW-based timing recovery scheme offers the best jitter performance in many situations[1]. One example is in a SONET/SDH/ATM network interface card application situation where TRU600A can be used between the O/E converter and a serial to parallel chip[2]. A summary of the specification follows:

Supply Voltage	**5 V**
Acquisition Time	**<2 ms**
Output Clock Random Jitter	**10 ps rms**
Power Consumption	**325 mW**

The TRU600 features a high-speed bipolar ASIC and a SAW filter in a hermetically sealed, 28-lead ceramic surface mountable package (18.5x10.5x3.4 mm3). To extract a clock signal from the input data, the data is first passed through a prefilter and frequency doubler stage. This generates pulses containing significant spectral energy at the input data rate. A precision narrow-band SAW filter, centered at the clock frequency, substantially suppresses jitter by rejecting other frequencies. The extracted clock is then accurately aligned with the incoming data signal at the input of a decision circuit which then retimes the data.

In addition to producing outputs with very low jitter, the TRU600 has excellent stability, fast acquisition time, and robust operation. It is available with standard SONET/SDH/ATM frequencies at 155.52, 311.04, and 622.08 MHz. Additional frequencies (124.416, 125, 139.264, 200, 265.625, and 278.528 MHz) for FDDI, ESCON, Fiber Channel, ISDN (CEPT 4), and other applications are also available.

To prepare for the increasing capacity demand in the tele/data communication market, a similar device which works up to the STS-48/STM-16 rate (2488.32 MHz) is being developed. Such a SAW-based clock and data recovery module is preferred in the emerging high speed optical communication receiver application[4].

1.2 Discrete SAW Filters for Timing Recovery

For customers who prefer to build their own timing recovery path on their SONET/SDH/ATM boards, we offer discrete SAW filters to perform the clock extraction function. They are available at 155.52, 622.08, and 2488.32 MHz. A summary of the specification follows:

Frequency (MHz)	**155.52**	**622.08**	**2488.32**
Insertion Loss (dB)	**17**	**15.5**	**19.5**
3-dB Q	**420**	**800**	**750**
Phase Slope (°/KHz)	**0.72**	**-0.33**	**-0.07**

The 155.52 MHz SAW filter is available in a standard 14-pin, metal dual-in-line package (20.3x12.7x7.4 mm^3). The 622.08 MHz SAW filter is available in a low-profile, 22-pin, metal surface mountable package (15.9x13.6x3.2 mm^3). The 2488.32 MHz SAW filter is available in a compact, surface mountable microwave package (11.4x10.7x2.1 mm^3). The 155.52 , 622.08, and 2488.32 Mhz timing recovery SAW filters are also available in the 9mmx7mm, 9mmx5mm, and 9mmx7mm leadless chip carrier surface mountable packages (LCC SMPs) respectively.

1.3 SAW-Based Voltage-Controlled Oscillator

The SAW-based voltage-controlled oscillator (VCO600) is a highly integrated device which uses an ASIC with an

9. Saw-Based Frequency Control Product Applications

on-chip phase shifter for frequency pulling and a SAW delay line with a typical 3-dB Q of 400. The VCO600 has an ECL output and is available with standard SONET/SDH/ATM frequencies at 155.52, 311.04, and 622.08 MHz. Additional frequencies at 278.528 and 368.64 MHz are also available. The VCO600 is housed in a hermetically sealed, 28-lead ceramic surface mountable package. Typical applications are data retiming and synchronization as part of a PLL, as well as frequency synthesis and frequency translation. The VCO600A also has a unique output disable and clock through feature which improves board-level testing. A summary of the specification follows:

Absolute Pull Range	**±50 ppm**
Supply Voltage	**-5 V**
Control Voltage	**-0.5 to -4.5 V**
Linearity	**±3%**
Spurious Output Suppression	**-60 dB**

2.1 SAW Filters for Wireless Applications

Wireless communication systems available include mobile cellular, cordless phones, paging services, Specialized Mobile Radio (SMR), mobile satellite and Wireless Local Area Network (WLAN). In Europe, the analog cellular system (ETACS) is being displaced by the new Global System for Mobile digital communication system (GSM). The Personal Handyphone System (PHS) and Personal Digital Cordless system (PDC) are gaining momentum in Japan (Table 1).

In the US, the existing analog cellular systems (AMPS) is being converted gradually into dual mode analog/digital systems (IS-54). Digital cellular system (IS-95) using the CDMA is also available in some metropolitan areas. These systems operate at the 800 MHz bands and claim to support more subscribers and provide better services. Non-licensed digital cordless phones using frequency hopping spread spectrum (FHSS) technique at the ISM-15 902-928 MHz band are in the market. They provide more secure services in the crowded consumer market of cordless phones. Paging companies are now providing two-way paging services. In-flight Air to Ground Telephony (AGT) service operating in the 849-851 MHz & 894-896 MHz bands is becoming more popular with the option to route ground to air calls. Wireless data transfer equipment (e.g. WLAN operating at the non-licensed ISM-15 2400-2483.5 MHz band) is now available[6]. SMR is changing into the enhanced version (ESMR) to support digital data/voice transport. Low/Medium Earth Orbit (LEO/MEO) Mobile Satellite Services like[5] IRIDIUM (Motorola), ARIES (Constellation Communication, Inc.), GLOBALSTAR (Loral & Qualcomm), ELLIPSAT (Ellipsat Corp.), Odyssey (TRW), and Teledesic (Microsoft et al.) will make "calling anyone, anytime, and anywhere" a reality. In addition, equipment using the Global Positioning System (GPS) technology is now available in the commercial (automobiles, aircrafts, ships, etc.) and consumer market (handheld receivers). Tremendous efforts are being put into developing low-power front end and baseband chips sets, longer life batteries, etc. In the RF and IF sections of the portable and stationary equipment of these systems, low-loss SAW filters and conventional high-loss and high-selectivity SAW filters have become and will continue to be the vital components[6]. Most European, US, and Japanese manufacturers of SAW filters are adding equipment and expanding their facilities to accommodate the business opportunities.

Table 1. World wide Wireless

Standard	Rx MHZ	TX MHz	#Users	RF BW MHZ	IF BW MHz
Analog Cellular (FDMA)					
AMPS	869-894	824-849	832	25	30
ETACS	916-949	871-904	1240	33	25
NTACS	860-870	915-925	400	10	12.5
NMRT450	463-468	453-458	200	5	25
NMT900	935-960	890-915	1999	25	12.5
Digital Cellular (TDMA)					
IS-54/-136	869-894	824-849	832X3	25	30
IS-95 (CDMA)	869-894	824-849	20X798	25	1250
GSM	935-960	890-915	124x8	25	200
PDC	810-826	940-956	1600x3	16	25
	1429-1453	1477-1501	1600x3	24	25
Digital Cordless/ PCN (TDMA/TDD)					
CT2 & 944/948	864/868 & 40		4	100	CT2+
DECT	1880-1990		10X12	110	1728
PHS	1907	1895	300X4	12	300
DCS1800 (FDD)	1805-1880	1710 1785	750X16	75	200

Telecommunication Standards

Continued

Table 1. World wide Wireless Telecommunication Standards

9. Saw-Based Frequency Control Product Applications

Standard	Rx MHZ	TX MHz	#Users	RF BW MHZ	IF BW MHz
Wireless Data-WAN/LAN (TDMA)					
CDPD	869-894	824-849	832	25	30
RAM	935-941	896-902	480	6	12.5
	403-470		450	67	12.5
Ardis	851-869	806-824	720	18	25
IEEE (US/Europe)	2400-2483	FHSS/79	83	1000	802.11
(CSMA)	2470-2499	DSSS/7	29	10000	(Japan)
Emerging Personal Communication System (PCS)					
	1930-1990	1850 1910		60	
High Tier (Larger Cell)					
PCS TDMA (based on IS-136 cellular)			Ericsson, AT&T, Hughes		
PCS CDMA (based on IS095 cellular)			Qualcomm, AT&T, Nokia		
PCS 1900 (based on GSM cellular)			Nortel, Ericsson, Nokia, Alcatel, Motorola, MCI, Pacific Telesis		
Wideband CDMA			InterDigital, OKI Low Tier (Small Cell)		
PACS (based on PHS Cordless)			Motorola, Panasonic, NEC, Hitachi Hughes, Bellecore		
DCT-U (based on DECT cordless)					
Composite CDMA/TDMA Omnipoint					

2.2 Low-Loss SAW Filters for Front-End RF Applications

The RF bandwidth in Table 1 shows the minimum bandwidth requirement for the front-end filtering in both the transmitting and receiving paths of different wireless systems. For many years, dielectric resonator filters (2 to 3 poles) have been widely used especially for the terminals. They are low cost, rugged, and easily implemented. In addition, they can handle high power. Though they were bulky, it was not a problem since early wireless terminals were mostly mobile but stationary (e.g. mounted in cars). However, the current trend of wireless equipment is moving toward more and more portable, and component size is one of the many factors that designers of terminals are concerned with.

Low-loss RF SAW filters (as low as 2.5 to 4 dB) between 800 and 1500 MHz are now available in LCCs as small as 3.8x3.8x1.6 mm^3 for AMPS, GSM, PDC, and other applications and the trend is moving toward 3.0x3.0x1.0 mm^3 for PCS, WAN, and WLAN, and other applications at 1.8 to 2.5 GHz band[7,8]. There are many suppliers of these devices from and Europe. Some of these companies offer robust products in this 800 to 1500 MHz range and are developing devices toward the 1.8 to 2.5 GHz range with the goal to attain even lower insertion loss. The popular designs are In-Line Coupled Resonator Filter (In-Line CRF, Figure 1) and Impedance Element Filter (IEF, Figure 2). The latter does not offer as good ultimate rejection and it can only be slightly improved by adjusting the capacitance ratio of the parallel and series arms. It does hold a good prospect in offering insertion loss lower than 2 dB with high frequency operation. Table 3 compares their applications and performance. Almost all low-loss RF SAW filters for mobile applications use $LiTaO_3$, $LiNbO_3$, or $Li_2B_4O_7$ as the substrate materials in order to provide the wide bandwidth requirement (up to 6%)[9].
One Japanese supplier recently announced the availability of SAW-based duplexers at the 800 MHz band

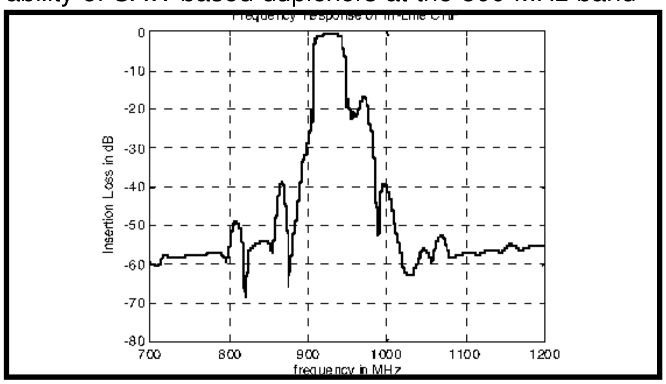


Figure 1. In-line CRF Design for RF Applications

has put itself as the leader of the pack[10]. They have succeeded in overcoming one major obstacle- power handling requirements for the transmission path in duplexer applications. In North America, only two suppliers manufacture RF SAW filters for cellular terminals and/or digital cordless phones (e.g. CT-2) and they are primarily captive.

Most low-loss RF SAW filter suppliers consider they have shrunk the footprints of the devices to small enough sizes. The trends are to put in efforts to reduce the package height possibly through flip-chip method[12] and, more importantly, to develop ways to further reduce the insertion loss to below 2 dB. The latter is to compete with the dielectric resonator filters which now have 1.3 to 3 dB insertion loss.

9. Saw-Based Frequency Control Product Applications

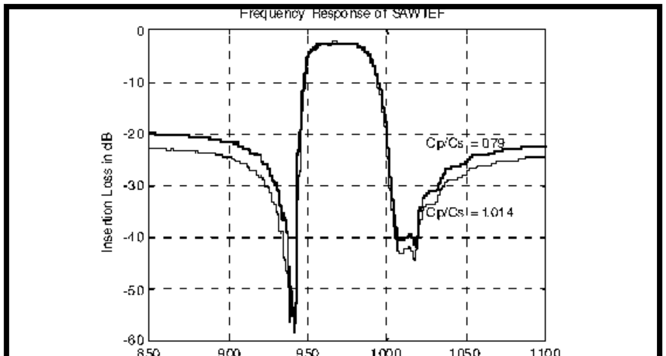


Figure 2. Impedance Element Filter Design for RF Applications

Many suppliers provide dielectric resonator filters, SAW filters, and chip monolithic LC-type filters to meet the frequency and bandwidth requirements for RF filtering. These devices are primarily different in insertion loss, attenuation, price, and size. Major progresses have been made in the development of chip monolithic LC-type RF filters and dielectric resonator filters[11]. The former has comparable size and insertion loss as SAW filters except they do not offer as good attenuation. Suppliers have also shrunk the size of dielectric resonator filters significantly in the last couple of years and it is a formidable competitor especially in the >2 GHz RF applications[12]. Table 2 depicts the generic comparison of these RF filter technologies.

	Dielectric Filter	SAW Filter	LC Multilayer Filter
Loss	Best	Good	Good
Attenuation	Good	Best	Good
Size (cubic mm)	Fair	Best	Good
Design Flexibility	Good	Fair	Best

Table 2. Generic Comparison of RF Filter Technology[11]

2.3 High Velocity Longitudinal Leaky SAWs and High Velocity SAWs in Piezoelectric Film/Diamond Structures

One way to maintain the physical feature size of transducer fingers while pushing up the operating frequencies is to increase the SAW velocity. LSAWs with low leakage loss are being used extensively in modern low-loss RF SAW filters. Popular LSAW cuts are 36° Y-X $LiTaO_3$, 41° and 64° Y-X $LiNbO_3$ [9]. LSAW's velocity is in general higher than that of the Rayleigh wave, and is always sandwiched in between the slow shear and fast shear velocities. They are attractive because of its high velocity, low leakage loss, and strong electromechanical coupling. In the last several years[13], we have seen progresses in the study of longitudinal LSAWs which have low leakage loss, strong electromechanical coupling, and comparable temperature coefficient of delay (TCD). It is foreseeable that wafer cuts using longitudinal LSAWs will become commercially available in the future to support high frequency SAW devices.

In the past several years, the synthesizing of polycrystalline diamond films using chemical vapor deposition (CVD) has become quite successful. In 1989, Yamanouchi et al. suggested theoretically that high frequency SAW devices (>3 GHz) could be realized in a piezoelectric AIN or ZnO/diamond structure because of the hardness of diamond film (Rayleigh wave velocity could exceed 12,000 m/s)[14]. Extensive experimental work is being actively pursued in Japan and Russia[15]. It's likely we will see vendors supplying diamond film coated SAW wafers in the future.

Design	TCRF	SPUDT	In-Line CRF	IRF
Application	IF	IF	IF & RF	RF
Current Frequency Range	<600 MHz	<400 MHz	<1GHz	As high as 2.4 GHz
Insertion Loss	>3 dB	6~10 dB	>2 dB	>1 dB
Bandwidth	0.04 to 0.1%	0.3 to 5%	0.08 to 5%	up to 6%
Materials	Quartz	Quartz & $LiTaO_3$ $Li_2B_4O_7$	Quartz, $LiTaO_3$, $LiNbO_3$ &	Quartz, $LiTaO_3$, & $LiNbO_3$
Strengths	Superior near-in rejection; Low-loss.	Superior out-of-band rejection.	Small size; Wide bandwidth; Traps placing is easy; Matching is not needed.	Small size; Wide bandwidth; Matching is not needed; Excellent near-in rejection.
Weakness is critical; Matching is generally needed	Metallization usually thick and uniformity is fingers usually needed; Difficult to Synthesize/ optimize	Matching is generally needed; long chip size; </8 direct transmission.	Sidelobe on high frequency side due to transducer frequencies.	Poor out-of band rejection Varied

Table 3. Comparison of Different Low-Less SAW Filter Designs for Current Applications

2.4 Low-Loss IF SAW Filters for Very Narrow Band Applications

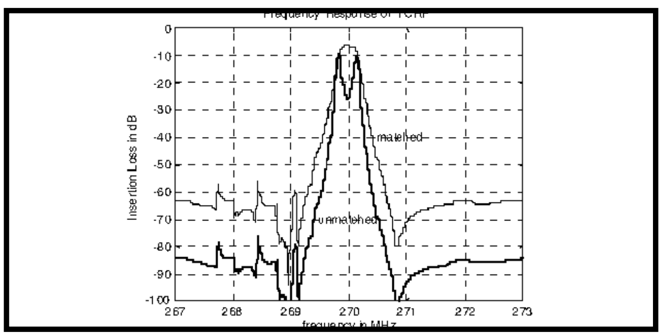
App Notes

9. Saw-Based Frequency Control Product Applications

The IF bandwidth listed in Table 1 depicts the channel width. For many years, 20 to 45 MHz monolithic crystal filters (MCFs) of 10 to 30 KHz bandwidth (4 to 6 poles) dominated the IF filtering segments of analog cellular systems like AMPS. Nowadays, the trend is to push up the IF frequency to help to suppress images and spurs due to mixing and the continuous narrowing of the transmitting and receiving bands in the RF carriers to support more channels[[16]] (e.g. the expansion of AMPS bands from 20 MHz to 25 MHz several years ago and the current expansion of GSM to EGSM). MCFs above 45 MHz, in addition to being fragile, are costly to make. Only one company from Japan is persistently pushing the MCFs to higher frequencies using the inverted mesa quartz resonator technique[[17]].

Figure 3. 4-Pole TCRF Design for IF Applications

Low-loss IF SAW filters at around 80 MHz for narrow



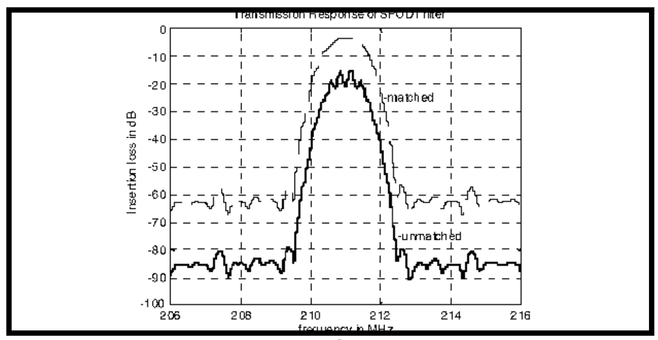
channel analog systems like AMPS applications employing the 4-pole Transversely-Coupled Resonator Filter design (TCRF, Figure 3) are now widely available. In addition to being low-loss (6 to 10 dB), these filters have excellent rejection in suppressing images after the mixing stage. It was also used as the RF front-end filter between 200 and 300 MHz in earlier narrow band pagers to allow down conversion directly to 455 KHz IF frequency without going through a first IF frequency of 21.4 MHz. Since the bandwidth is very narrow, quartz SAW substrate is exclusively used to minimize frequency drift due to temperature. Standard frequencies at 82.2, 83.16, 85.05, 86.85, and 90 MHz are available. 13.3 x 6.5 x 1.3 mm^3, 15.4 x 6.5 x 1.5 mm^3, and other LCCs are widely used. There are many suppliers of these "standard" filters from Japan and Europe.

2.5 Low-Loss IF SAW Filters for Narrow Band Applications

IF filtering in digital cellular systems usually requires wider bandwidth and stringent delay characteristic. Single-Phase Unidirectional Transversal SAW filter (SPUDT) is one of the few designs used to achieve the bandwidth and delay requirements for the digital systems. The SPUDT design ingeniously directs power transmission from the electrical port to the forward acoustical port by setting a certain phase shift (±45° or ±135°) between the transduction center and the reflection center. When the matching of the electrical port begins, the insertion loss will decrease (Figure 4). The triple transit echo will also decrease (reflection coefficient decreases) as the acoustical reflection and the piezoelectric regeneration begin to cancel out.

Figure 4. SPUDT Design for IF Applications

Comparing with the conventional transversal filter design which has only a transduction function to work



with, the challenge for the SPUDT design is now one has to properly account for the reflection function also. The In-Line CRF design described in the low-loss RF SAW filters section can also be used to provide even wider bandwidth than the SPUDT design in IF applications (Figure 5). Table 3 compares their applications and performance. Depending on the requirements, devices in LCCs with footprints anywhere from 5 x 5mm^2 to 19 x 6.5mm^2 are available.

Similar to the analog systems like AMPS (or IS-54), we begin to see standardized IF frequencies in some popular digital wireless terminals (e.g. 71 MHz for GSM, 110.592 MHz for DECT, 130 MHz for PDC, 248.45 MHz for PHS et al.). Same as the low-loss RF SAW filters, suppliers of these standard low-loss IF

SAW filters are usually more bulky and costly than the low-loss RF SAW filters. Many designers are seeking ways to reduce the size as a means to reduce the

9. Saw-Based Frequency Control Product Applications

cost[18]. In-Line CRF design can usually fit into smaller packages than the SPUDT design and circuit matching is in general not needed.

Most IF filterings in emerging systems though, are implemented differently; very much dependent on the system designers. In the US there are tremendous needs of SAW filters to perform IF filtering for different new wireless equipment (terminals and base stations) based on the newly allocated PCS bands. These new systems will be operating at the 1.8 to 2.0 GHz range. The equipment will very likely need to down convert the radio signals to IF frequency (50 to 500 MHz) for processing.

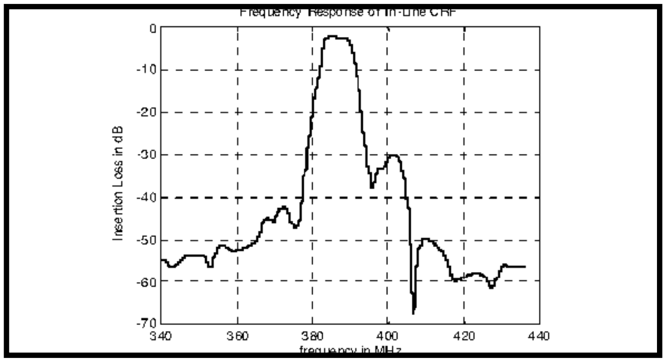


Figure 5. In-Line CRF Design for IF Applications

2.6 SAW Filters for CDMA Base station Applications

The technique of using direct sequence spread spectrum method in providing multiple access to frequency channels (CDMA) is gaining momentum worldwide. In the US, IS-95 regulates the usage of this technology for cellular applications in the 900 MHz range. New systems using the CDMA will appear in the PCS band.

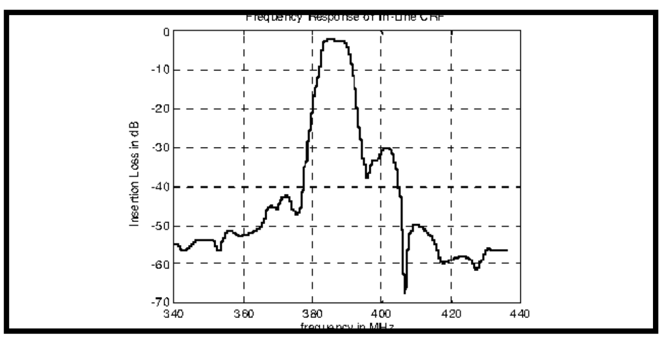


Figure 6. Frequency Response of a 131.01 MHz SAW Filter for CDMA Base station Applications

Conventional SAW filters, though high in insertion loss, offer unsurpassed selectivity (low shape factor) and high rejection. They begin to find extensive applications in the terminals and base station of existing and emerging systems[19]. One example is a 131.01 MHz SAW filter for IF filtering in CDMA base station (Figure 6). Quartz substrate is used for such a device in order to meet the 1.25 MHz channel width requirement over temperature. For many emerging CDMA systems (e.g. W-CDMA), SAW filters will probably continue to be the only solution which can provide robust filtering function in the IF segment.

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10. Evacuated Miniature Crystal Oscillators (EMXO™)

Vectron International Announces a Technological Breakthrough in Oscillator Design by Introducing our Evacuated Miniature Crystal Oscillator (EMXO™)

OCXO's (Oven Controlled Crystal Oscillators) are used when frequency vs. temperature requirements are too stringent to be met by a basic XO (Crystal Oscillator) or TCXO (Temperature Compensated Crystal Oscillator). With an OCXO, the temperature of the crystal and critical circuits is kept constant as the temperature outside the oscillator varies. Controlling the temperature inside the oscillator with an oven maintains this constant temperature. In an OCXO, the changes in the ambient temperature are sensed and then fed back to an oven control that continually maintains a constant optimum temperature inside the oscillator enclosure. An OCXO can improve the crystal's inherent stability by more than 5000 times. The oven control system is not perfect, the open loop gain is not infinite, there are internal temperature gradients inside the oven (oscillator) and, in a conventional oven, the circuitry outside the oven shell is subjected to ambient temperature changes that can "pull" the frequency.

The improved temperature stability performance of a conventional OCXO over an XO or TCXO comes at a steep price. OCXO power consumption, for instance, is greater by a factor of over 200. There is also a size consideration. In an ordinary OCXO, a crystal is enclosed in a metal case, which is then placed inside an oven shell together with temperature sensitive circuitry, and then surrounded by thermal insulation. All this, plus any additional circuitry are then placed in a metal housing making for a bulky package, which becomes very difficult to miniaturize.

To overcome these obstacles, the EX-380 Series EMXO (Evacuated Miniature Oven Controlled Crystal Oscillator) was specifically developed to achieve OCXO performance while significantly lowering power consumption and reducing package size (See Figure 1).

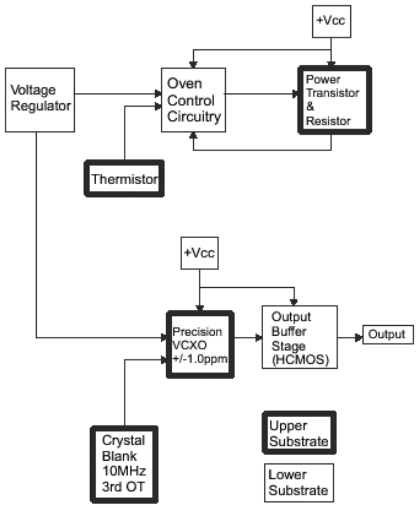

Figure 1. EX-380 Functional Block Diagram

These characteristics go hand in hand since reducing package size makes it easier to improve power consumption. First, the volume of the package was made as small as possible to reduce the volume that the oven needs to heat. Secondly, the most effective insulation needed to be used. In the EX-380 Series, Vectron has done both. The package was designed to single DIP dimensions of 0.82" x 0.52" x 0.3", and the oscillator uses a vacuum as the insulation medium - a dramatic improvement over conventional polyfoam or fiber based insulation material. Another great contributor to Vectron's efforts to reduce size and still provide "oven oscillator" performance was to eliminate the use of large packaged crystals which, up until now, had to be used to achieve good aging. Instead, a way to use an open crystal blank was found and made practical. Vectron has succeeded in resolving outgassing and contamination issues, which could degrade performance. To do this required manufacturing the oscillator with a high internal vacuum level, with low internal outgassing, to provide the needed thermal insulation. A high level of cleanliness was needed to prevent contamination of the open (un-encased) crystal blank and to ensure exceptional long term crystal aging.

The key design feature of this package utilized the concept of integrating the precision crystal in blank form in combination with hybrid microelectronics circuitry. In doing this, obtaining good aging performance was paramount. For this reason, a cold welded pack-

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10. Evacuated Miniature Crystal Oscillators (EMXO™)

age was chosen rather than a more traditional resistance welded package. Cold weld sealing provided a true metallurgical bond between ductile metal surfaces without added heat from the sealing process. Under the high tonnage pressure introduced through the indentation of the welding die, a plasticity flow of material takes place on the mating surfaces. The end result is a hermetically sealed enclosure without contamination from weld splashes, dust and vapors. And, most important, cold weld sealed enclosures achieves a high level of vacuum integrity.

Mechanically, the hybrid circuit and crystal assembly is suspended directly over a highly insulating structure to minimize heat energy loss through conduction. In addition, the entire assembly is thermally insulated to the enclosure by vacuum at a pressure level of 10-6 torr. Based on the steady state thermal conduction calculation, this package design resulted in a thermal resistance of >300 degrees C/watt.

The EMXO manufacturing process is interesting and a process flow diagram is shown below in figure 2.

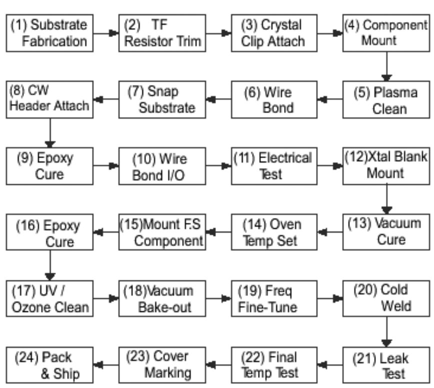
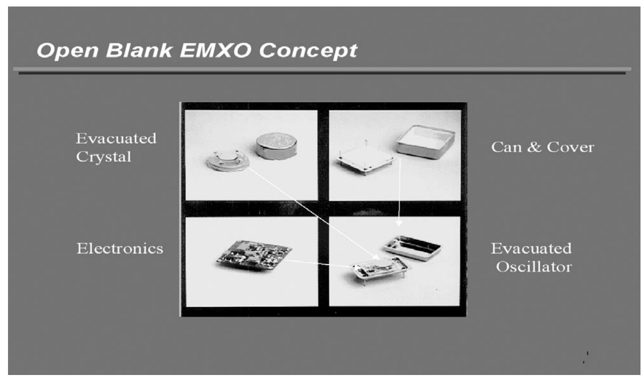


Figure 2. EMXO Process Flow Diagram

Substrates are fabricated with thick film screen printing techniques with each deposition layer subjected to three different process stages - print, dry and fire. Crystal clips are attached to the gold conductor trace on a substrate with high thermal conductivity. All active and passive components are mounted on the substrate using a conductive adhesive and then moved to a convection oven for curing. After the cure process, the hybrid is cleaned to remove organic and non-organic contaminants. Wires are bonded on the hybrid circuit as interconnects. The hybrid circuits are then attached to the cold-weld package with adhesive. Finally, blank crystals are mounted onto the clips and tuned to the nominal frequency needed, by an evaporation process, to a typical accuracy of 1 ppm. The units are then cold weld sealed. The oven itself is heated by direct thermal conduction applied to a heat conductive substrate.

This "Open Blank" EMXO concept is shown and compared to conventional OCXO construction, in Figure 3 below.



In figure 3 above, 1,2 and 3 reflect conventional OCXO construction while 4 is the EMXO. It shows the major elements of the SDIL EMXO. Only one substrate is used and all the elements are heated. The oscillator is essentially a CMOS gate type with an additional varactor diode and LC trap for overtone select. The resonator is a 3rd Overtone, doubly rotated cut as required by the application, both of which offer superior aging performance when compared to a traditional fundamental resonator.

It is anticipated that the EX-380 Series will find applications where performance in severe mechanical environments is equally important to electrical performance. An additional focus for the EX-380 series, therefore, was to provide robust construction to withstand high shock and vibration and to yield good G-sensitivity performance. For example, when the physical orientation of an oscillator is changed, there is a small frequency change (typically not more than several parts in 10-9 for a 90-degree rotation) due to change in stress on the crystal blank resulting from the gravitational effect upon the crystal supports. This characteristic is known as "tip-over" and is expressed in 10-9/g where one g represents one-half of a 180-degree orientation change. To minimize this change

10. Evacuated Miniature Crystal Oscillators (EMXO™)

and also to enhance performance under shock and vibration, the crystal blank is mounted in a symmetrical mounting structure, instead of the more traditional 2 or 3 points. This helps to achieve a high shock and vibration endurance level, low g-sensitivity performance and symmetrical heat transfer. Also, when a crystal oscillator is operating and subjected to vibration, spurious frequencies are generated, offset from the frequency of oscillation by the frequency of vibration. These are commonly referred to as "vibration induced side-bands" and these side bands behave similarly to phase noise. The amplitude of these spurious outputs is related to the amplitude of vibration, the mechanical design of the crystal supports, and the mechanical design of the oscillator assembly, including the crystal mounting. Here also the symmetrical crystal mounting structure helps to reduce unwanted noise.

Even though many types of doubly rotated crystals produce lower amplitude spurii under vibration than AT cut crystals, this characteristic is primarily determined by the mechanical design of the crystal and oscillator rather than the specific crystal cut. Vectron uses a doubly rotated resonator in the EMXO series oscillator to provide lower close in phase noise, better aging rates and reduced acceleration sensitivity. Figures 4 through 10 represent the typical actual test data on qualification samples for various characteristics.

Figure 4

Frequency vs Temperature Characteristics EX-380 SERIES @ 10 MHz (Typical)

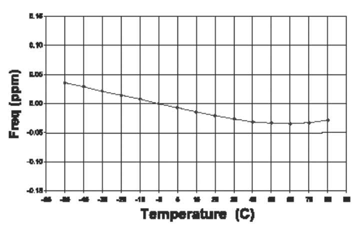


Figure 5

Warm-up (Restabilization) Characteristic at +25ºC

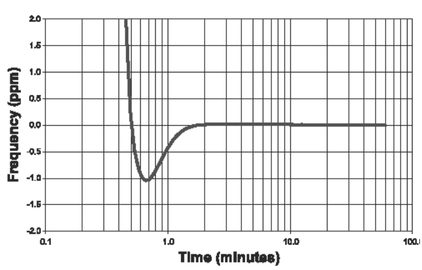


Figure 6

This is a typical phase noise plot for the EX-380 series at 10 MHz. Significant phase noise improvement, both close in and at the noise floor, can be obtained on special order.

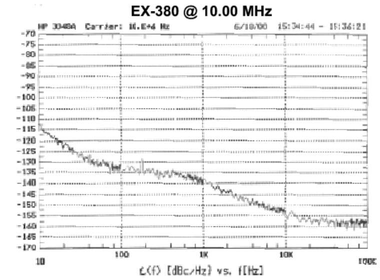


Figure 7

Frequency vs Supply Voltage (Typical)

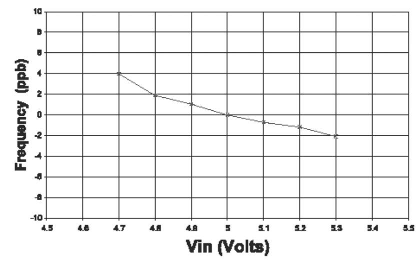


Figure 8

Pullability Characteristic. Frequency Change vs Control Voltage Input

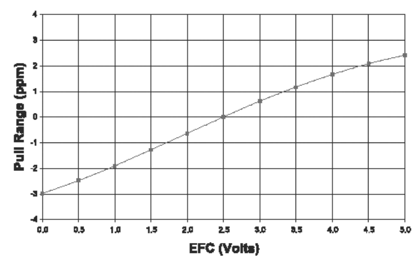


Figure 9

Steady State Current vs Ambient Temperature at 10 MHz (Typical)

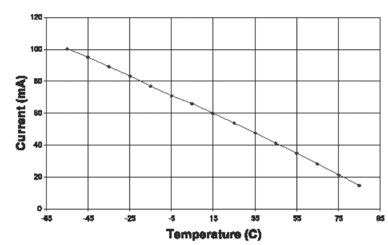
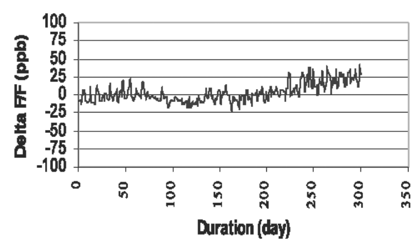


Figure 10

Frequency vs Time. aging plot @ 10 MHz (Typical)



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10. Evacuated Miniature Crystal Oscillators (EMXO™)

Summary:

The model EX-380, low profile 4 Pin DIP Evacuated Miniature, Oven Controlled Crystal Oscillator (EMXO) is available at selected frequencies from 10 MHz to 80 MHz.

The unit provides exceptionally low aging rates and high temperature stabilities in an extremely small package over a wide range of environmental conditions. The through hole unit measures only 20.8mm x 13.2mm x 7.6mm (0.82" x 0.52" x 0.30"), provides aging rates of <1x10-9 /day average, <1x10-7 for the first year and <1x10-6 for 10 years with temperature stabilities to ±1x10-7 over -40ºC to +85ºC. Wider temperature ranges are available from -55ºC to +85ºC. This performance is achieved by the application of new resonator design concepts and technological breakthroughs. The EMXO bridges the gap between current large, high precision OCXO's and smaller TCXO's and becomes the most economical choice where there is a need for spectral purity, short and long term stability, along with small size and dramatically reduced power consumption.

Standard supply voltages for the EX-380 series are 3.3 Vdc and 5 Vdc, all with an HCMOS, Complementary PECL, LVDS and sinewave output. A surface mount version of this oscillator is available (EX-381/4/5). Sinewave output of 0 dBm to +3.0 dBm / 50 ohm is available in the EX-381 surface mount version. LVDS and complementary PECL are available in the EX-384 surface mount version and HCMOS is available in the EX-385 surface mount version.

These EMXO units are ideal for SONET/SDH, DWDM, FDM, ATM, 3G, Telecom Transmission and Switching Equipment, Wireless Communication Equipment and Military Airborne and Mobile systems.