A Nonlinear *S*-parameters Behavioral Model for RF LNAs

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Abstract

A nonlinear behavioral model for radio frequency low noise amplifiers (LNA's) is presented. The model captures effects of nonlinearity, output power saturation, noise figure and port impedance mismatch. A high-level *S*-parameters approach is adopted during the model derivation. Consequently, the model inherits the *S*-parameters dual ability to characterize the transfer function between ports while including their impedances. The model derivation is thoroughly discussed showing how the effects of intermodulation as well as output power saturation can be included within the *S*-parameters representation for the block. Furthermore, in order to minimize the calibration effort, the model generics are made such that they map directly to typical LNA specifications. It follows that the model as implemented is not topology specific and can be easily calibrated to serve within top-down or bottom-up verification flows. Finally, the model accuracy is validated against reference transistor level simulations. Results comparison shows good agreement is attained.

Keywords

Behavioral model, intermodulation, LNA, non-linearity, radio-frequency, *S*-parameters.

1. Introduction

System-on-chip verification continues to grow driven by the increasing level of integration of functionalities to embed in a single die. Depending on the system architecture and the verification methodology, one may need to perform top level simulations that often involve digital/RF/analog types of signals. In this case, full transistor-level representation becomes impossible to serve where SPICE capacity limitation has been known to be the major impediment. To overcome this limitation, behavioral modeling is conveniently used to complete the task.

During a typical verification plan, the objectives targeted determine the complexity level of the behavioral models engaged. In particular, analog/RF modeling as opposed to digital modeling, requires a wide variety of skills. For instance, analog modeling necessitates a deep understanding for the block operation. Additionally, while abstracting the behavior, assumptions should be carefully made in order to stay aligned with the verification objectives. Moreover, the behavior needs to be mathematically formulated in a form that facilitates convergence by numerical solvers.

Literature has shown different approaches adopted to tackle the modeling of the LNA block. In [1], a high-level accurate model for weakly non-linear narrowband LNA is implemented in Verilog-A. Conversely, a VHDL-AMS library of RF blocks is demonstrated in [2] where the $IP3$ and NF were neglected despite their relevance as important RF metrics. Others like [3] and [4], use a semi-structural approach to include frequency dependence and deploy optimization for model calibration.

This work envisions the high-level behavior of the LNA using an *S*-parameters approach. While similar to the stand point presented in [5], a more detailed analysis is presented here with emphasis on how non-linearity can be lumped into the *S*-parameters representation. The outcome of the analysis is a versatile model that is not topology specific. In addition, the model can be fully calibrated using physical generics that map one-to-one to LNA typical specifications. During the analysis, assumptions together with their validity and implications are also discussed.

The analysis starts in Section 2 by defining the variables describing an arbitrary 2-port *S*-parameters linear network. Next, non-linearity in the output voltage equation is mapped to the *S*-parameters domain and expressed in terms of the intermodulation distortion specs $(IP2, IP3)$. Subsequently, we demonstrate how the output power can be smoothly saturated and discuss the implications of the implementation within the model. Furthermore, we show how the model can be adapted to include the complex nature of the input/output impedances. Noise figure modeling follows in Section 3. Section 4 gives quick highlights on the VHDL-AMS source code as listed in Appendix A. Our model is next compared to transistor-level simulation for a given LNA topology in Section 5. Finally, Section 6 concludes with a briefing summary.

2. Modeling analysis

2.1. A linear 2-port *S*-parameters model

We start by defining a linear model for an arbitrary 2-port network. Figure 1, below, depicts an equivalent *S*-parameters representation. Port 1 is assumed to be the input port where the incident and reflected waves are denoted by a_1 and b_1, respectively. Following the same convention, a_2 and b_2 are defined at port 2 which denotes the output port. Using [6], one can relate a_1, a_2, b_1 and b_2 to their corresponding voltages and currents to obtain

$$a_1 = \frac{1}{2\sqrt{Z_{o1}}}\left(V_1 + I_1 Z_{o1}\right), \quad (1)$$

$$b_1 = \frac{1}{2\sqrt{Z_{o1}}}\left(V_1 - I_1 Z_{o1}\right), \quad (2)$$

$$a_2 = \frac{1}{2\sqrt{Z_{o2}}}\left(V_2 + I_2 Z_{o2}\right), \quad (3)$$

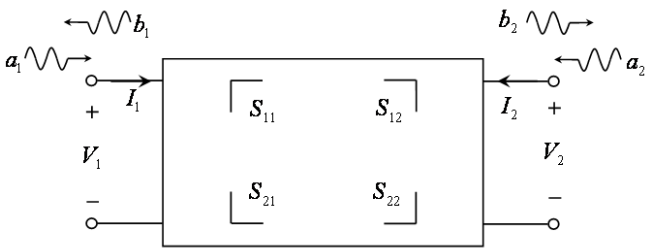

Figure 1: Two port *S*-parameters representation.

$$b_2 = \frac{1}{2\sqrt{Z_{o2}}}(V_2 - I_2 Z_{o2}), \tag{4}$$

where Z_{o1} and Z_{o2} are the characteristic impedances for ports 1 and 2, respectively.

In addition, the above quantities are also inter-related through the block specific *S*-parameters as follows:

$$b_1 = S_{11}a_1 + S_{12}a_2, \tag{5}$$

$$b_2 = S_{21}a_1 + S_{22}a_2. \tag{6}$$

In this case, after applying the source and load conditions, the system can be solved for (V_1, I_1) and (V_2, I_2).

2.2. Non-Linearity Modeling

In general, a 2-port network exhibiting non-linearity produces an output voltage V_2 that can be related to the input voltage V_1 by

$$V_2 = c_1 V_1 + c_2 V_1^2 + c_3 V_1^3, \tag{7}$$

where c_1 represents the voltage gain linear term while c_2 and c_3 are the non-linear gain coefficients. In this case, one may also express the transmitted wave b_2 in a similar non-linear form using

$$b_2 = S_{21}a_1 + k_2 a_1^2 + k_3 a_1^3 + S_{22}a_2. \tag{8}$$

At this point, it is useful to relate between the *k*'s and *c*'s coefficients using the intermodulation distortion analysis. Under the latter condition, port 2 is matched and $a_2 = 0$. It follows that Eq (5) together with Eq (1) and (2) yield

$$V_1 = \sqrt{Z_{o1}}\left[a_1(1 + S_{11})\right]. \tag{9}$$

Similarly, Eq (3) and (4) give

$$V_2 = \sqrt{Z_{o2}}\, b_2. \tag{10}$$

We can now substitute from Eq (7), (8) and (9) into (10) to formulate the relationship between the two sets of coefficients which can be expressed as follows:

$$S_{21} = \sqrt{\frac{Z_{o1}}{Z_{o2}}}(1 + S_{11})\ c_1, \tag{11}$$

$$k_2 = \sqrt{\frac{Z_{o1}}{Z_{o2}}} Z_{o1}^{1/2}(1 + S_{11})^2\ c_2, \tag{12}$$

$$k_3 = \sqrt{\frac{Z_{o1}}{Z_{o2}}} Z_{o1}(1 + S_{11})^3\ c_3. \tag{13}$$

Or more generally, for n = [1, 2, 3,…], we have

$$k_n = \sqrt{\frac{Z_{o1}}{Z_{o2}}} Z_{o1}^{(n-1)/2}(1 + S_{11})^n\ c_n. \tag{15}$$

Subsequently, one can use the second and third order intermodulation distortion conditions [7] to determine the dependence of k_2 and k_3 on the second order input intercept P_{IIP2} and the third order input intercept P_{IIP3}, respectively. In this case, the second order intermodulation distortion dictates

$$c_2 = -\frac{c_1}{A_{IIP2}}, \tag{16}$$

where $V_1 = A_{IIP2}$ is the input signal amplitude at the second order intercept point. At this condition, one may also write

$$P_{IIP2} = \frac{A_{IIP2}^2}{2Z_{IN}}, \tag{17}$$

where $Z_{IN} = Z_{o1}\dfrac{1 + S_{11}}{1 - S_{11}}$. (18)

Using Eq(11, 12, 17, 18) into (16), one can express k_2 as

$$k_2 = -\sqrt{\frac{1 - |S_{11}|^2}{2P_{IIP2}}}\, S_{21}. \tag{19}$$

Similarly, applying the same procedure while using Eq(13), k_3 is given by

$$k_3 = -\frac{2}{3}\frac{\left(1 - |S_{11}|^2\right)}{P_{IIP3}} S_{21}. \tag{20}$$

The analysis as concluded above by Eq(19, 20) can now be used to develop a generic behavioral model for an arbitrary non-linear two port network. The model core consists of the series of Eq(1-5) in addition to Eq(8, 19, 20). If follows that the *S*-parameters and the input 2nd and 3rd order intercepts $(P_{IIP2},\ P_{IIP3})$ become the input generics to the model. This formulation is useful as the model can be easily calibrated using generics that directly map to the system level specifications.

2.3. Output power saturation effect

In the previous analysis, the non-linear terms were truncated thus limiting the distortion effects up to the third order. This approximation is found sufficient to model the amplifier non-linearity up to power levels near the 1dB compression point [7]. At slightly higher input power levels, third order non-linearity is unable to limit the output power level and therefore the model becomes inaccurate in this region.

In general, this region is not of common interest and typical operation is recommended within the safe dynamic range of the amplifier. However, increasing the validity range of the model may turn beneficial when operation is sometimes pushed near the limit and accuracy is required to be maintained. In these occasions, a more comprehensive behavioral model is appreciated since it still mimics the amplifier real behavior at a cheap CPU cost.

To saturate the output power, one could argue that it could be achieved by applying a limiting function to the

output voltage (or current). Nevertheless, this will significantly alter the output impedance of the amplifier potentially harming subsequent connected blocks.

Instead, we decided to model the output saturation effect by limiting the input power level transmitted to the system. Realizing the fact that this would harm the input impedance, an additional free[1] quantity V_{1_EFF} was defined such that

$$\begin{aligned} V_{1\_EFF} &= V_1 && \text{for } |V_1| < V_{1\_\max} \\ &= +V_{1\_\max} && \text{for } V_1 > +V_{1\_\max} \\ &= -V_{1\_\max} && \text{for } V_1 < -V_{1\_\max} \end{aligned} \tag{21}$$

where $V_{1\_\max} = \sqrt{2P_{1\_\max}Z_{in}}$ and $Z_{in} = Z_{o1}\frac{1+S_{11}}{1-S_{11}}$. In addition, from [7], we may set $P_{1\_\max} \cong P_{1dB\_comp} \cong P_{IIP3} - 9.6dB$. At the same time, the input impedance is preserved using

$$V_1 = I_1 Z_{in} = I_1 Z_{o1}\frac{1+S_{11}}{1-S_{11}}. \tag{22}$$

Consequently, the rest of the model equations are given by

$$a_1 = \frac{1}{2\sqrt{Z_{o1}}}\left(V_{1\_EFF} + I_{1\_EFF}Z_{o1}\right) \tag{23}$$

$$b_1 = \frac{1}{2\sqrt{Z_{o1}}}(V_{1\_EFF} - I_{1\_EFF}Z_{o1}) \tag{24}$$

$$a_2 = \frac{1}{2\sqrt{Z_{o2}}}\left(V_2 + I_2 Z_{o2}\right) \tag{25}$$

$$b_2 = \frac{1}{2\sqrt{Z_{o2}}}(V_2 - I_2 Z_{o2}) \tag{26}$$

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{27}$$

$$b_2 = S_{21}a_1 + k_2 a_1^2 + k_3 a_1^3 + S_{12}a_2 \tag{28}$$

Note that Eq(23) and Eq(24) introduce an additional free quantity I_{1_EFF} that gets implicitly computed within the system depending on V_{1_EFF} and Z_{in_EFF} where the latter quantity is the input impedance of the system given by

$$Z_{in\_EFF} = Z_{o1}\frac{(1+S_{11})(1-S_{22}\Gamma_L)+S_{12}S_{21}\Gamma_L}{(1-S_{11})(1-S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_L}, \tag{29}$$

Γ_L being the reflection coefficient at the load.

Comparing Eq(29) and Eq(22), one may realize that in this case, the input impedance Z_{in} as seen at the physical input port of the model is approximate since it assumes that the device is unilateral $(S_{12} = 0)$ and/or that reflections at the load are small enough $(\Gamma_L \cong 0)$. In practice, the latter conditions are true to a degree that is sufficient to justify the validity of our assumption.

Finally, it remains to mention that the limiting conditions as cited in Eq(21) are better implemented using a single continuous function to avoid convergence difficulties encountered by numerical solvers. Such a function is normally chosen to provide a smooth transition between the different regions. Nevertheless, in our case, this function should be selected with extra care as it may introduce additional non-linearity thereby upsetting the previously included P_{IIP2} and P_{IIP3}. For this reason, the *hyp* function [8] is selected and is generally expressed as

$$hyp_1(x,\delta) = \frac{1}{2}\left(x + \sqrt{x^2 + 4\delta^2}\right). \tag{30}$$

Note that parameter δ in the above expression provides a precise control over the smoothness at the transition edges. Minimizing δ will guarantee the contribution of the *hyp* function to the overall non-linearity of the amplifier remain negligible hence original distortion effects will not be affected.

It can be noted however that the hyp_1 type function as expressed in Eq(30) provides a single smooth transition edge at $x = 0$. This equation can be further manipulated to provide a double smooth transition at $\pm V_{1\_\max}$ using

$$V_{1\_\text{int}} = V_1 - 0.5\left[\left(V_1 + V_{1\_\max}\right) - \sqrt{\left(V_1 + V_{1\_\max}\right)^2 + 4\delta^2}\right], \tag{31}$$

$$\begin{aligned} V_{1\_EFF} = V_{1\_\text{int}} - 0.5\Big[&\left(V_{1\_\text{int}} - V_{1\_\max}\right) \\ &+ \sqrt{\left(V_{1\_\text{int}} - V_{1\_\max}\right)^2 + 4\delta^2}\Big], \end{aligned} \tag{32}$$

where V_{1_int} is an intermediate free quantity that enables the usage of the *hyp* function recursively. Figure 2 depicts the overall resulting relationship between V_{1_EFF} and V_1 with $\delta = 1e-9$ and $|V_{1\_\max}| = 2.0$.

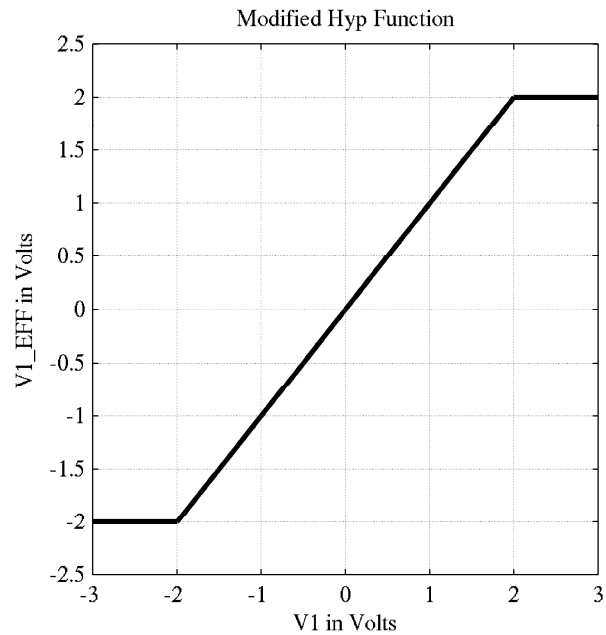

Figure 2: Saturation behavior between V_{1_EFF} and V_1 using a recursive hyp_1 function.

2.4. Noise figure modeling

To model the noise figure of the LNA, we first realize that the behavioral model equations as previously discussed

[1] A *free* quantity does not relate to any voltage or current of a physical port.

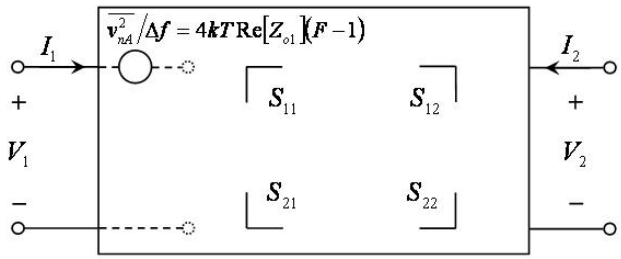

Figure 3: Noise Figure effect added to the LNA behavioral model.

are generally considered as noiseless by a SPICE environment. It follows that even though the input impedance of the LNA includes an implicit resistive part, the latter is not treated as a noise source during a regular SPICE noise analysis.

Consequently, to lump in the input referred equivalent noise added by the LNA, we define a voltage noise source whose power spectral density (V^2/Hz) is defined by

$$N_A = \frac{\overline{v_{nA}^2}}{\Delta f} = (F-1)N_S, \tag{33}$$

where N_S is the thermal noise contribution from the source equal to $4kT\,\mathrm{Re}[Z_{o1}]$. Figure 3 shows how the N_A source is connected to the model to ensure its contribution is added to the noise introduced by the source. Moreover, for other types of SPICE analysis, the voltage noise source acts as a short circuit thus preserving the original operation of the block.

2.5. Complex input/output impedance modeling

In the above discussion, the input and output impedances of the LNA were characterized using the corresponding *S*-parameters in their magnitude form. In practice, RF designers will find it more useful to account for the complex nature of the ports. This effect can be incorporated within our previously developed analysis as discussed hereafter.

First, we assume the input impedance of the LNA can be represented by an equivalent network comprising of R_1 in parallel with C_1. Assuming the device is unilateral, one may write

$$I_1 = \frac{V_1}{R_1} + C_1\frac{dV_1}{dt}. \tag{34}$$

Subsequently, as discussed in Section 2.3, one may define new free quantities $(V_{1\_EFF},\ I_{1\_EFF})$ such that V_{1_EFF} and V_1 are related through Eq(31) and (32). Again, exploiting the unilateral assumption, one may relate V_{1_EFF} and I_{1_EFF} using

$$I_{1\_EFF} = \frac{V_{1\_EFF}}{R_1} + C_1\frac{dV_{1\_EFF}}{dt}. \tag{35}$$

On the other hand, to include the complex output impedance, we represent it by the parallel combination of R_2 and C_2. Moreover, we use

$$I_2 = \frac{1}{\sqrt{Z_{o2}}}(a_2 - b_2). \tag{36}$$

Substituting from Eq (28) into Eq (36), we get

$$I_2 = \frac{1}{\sqrt{Z_{o2}}}\left[a_2(1-S_{22}) - \left(S_{21}a_1 + k_2a_1^2 + k_3a_1^3\right)\right]. \tag{37}$$

For $S_{12} = 0$, we have

$$S_{22} = \frac{Z_2 - Z_{o2}}{Z_2 + Z_{o2}}, \tag{38}$$

where $\frac{1}{Z_2} = \frac{1}{R_2} + sC_2$.

From Eq (38, 25) into (37) and after rearranging, one may relate I_2 and V_2 to obtain

$$\begin{aligned} I_2 &= \frac{V_2}{R_2} + C_2\frac{dV_2}{dt} \\ &- \sqrt{Z_{o2}}\left[S_{21}a_1 + k_2a_1^2 + k_3a_1^3\right]\left[\frac{1}{Z_{o2}} + \frac{1}{R_2}\right] \\ &- \sqrt{Z_{o2}}C_2\left[S_{21}\frac{da_1}{dt} + k_2\frac{da_1^2}{dt} + k_3\frac{da_1^3}{dt}\right] \end{aligned} \tag{40}$$

where a_1 is still given by Eq (23). Eq (40) is therefore used to determine the non-linearity exhibited by the output power while maintaining a complex output impedance. At the same time, a_1 will still lead the output power to saturate since it is given as a function of $(V_{1\_EFF},\ I_{1\_EFF})$.

3. VHDL-AMS source code

The behavioral model was developed in VHDL-AMS and the source code is given in Appendix A. The input port (port 1) is defined between terminals ain and ground whereas the output port (port 2) is defined between terminals aout and ground. Nomenclature consistency is retained in the source code development for direct comparison between the code and the previous analysis. It can also be noted that the noise source quantity was implemented using an Eldo/SPICE component instantiation for a voltage noise source where the ambient temperature is parsed as a generic.

4. Behavioral model versus transistor level simulations

To verify the accuracy of the previous analysis, a simulation comparison is conducted between an arbitrary transistor level LNA and its corresponding behavioral model as previously devised. Figure 4 shows the schematic for the LNA topology in question.

In order to calibrate the behavioral model, typical testbenches were first created to characterize the LNA block in terms of its *S*-parameters and non-linearity. RF simulations were conducted using EldoRF™ [9]. Table 1 summarizes the performance metrics for the tested design.

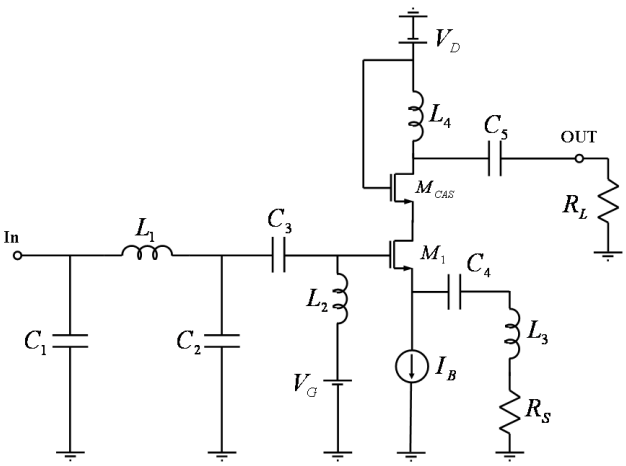

Figure 4: LNA transistor level circuit.

Table 1: Summary of LNA design parameters.

Parameter	Value
Technology	0.25µm CMOS
f_o	2.45 GHz
S_{11}	-15.64 dB
S_{21}	15.27 dB
S_{12}	-34.12 dB
S_{22}	-1.23 dB
Z_{o1}	50.0 Ω
Z_{o2}	200.0 Ω
R_{IN}	69.78 Ω
C_{IN}	191.42 aF
R_{OUT}	1.91 kΩ
C_{OUT}	224 fF
$IIP2$	5.23 dBm
$IIP3$	1.23 dBm
NF	1.4 dB

The above parameter values were then assigned as generics to the *S*-parameters based model as well as its *RC* counterpart. Next, the testbenches were reused inside Questa ADMSRF™ [10] and results were compared against transistor level simulations. Figure 5 depicts such comparison in terms of power gain. It is clear that results are in good agreement with a maximum absolute error of ~0.7dB at an input power of ~-10 dBm. In addition, the extracted 1 dB compression point at the input using the model is -9.13dBm versus -11dBm using transistor level simulation. Moreover, the P_{IIP2}, P_{IIP3} and NF were verified to be identical to the transistor level results thus showing the adequacy of the analysis.

6. Conclusion

A behavioral model for an RF LNA has been developed based on an *S*-parameters approach. The analysis as devised, is not topology specific and lumps the non-linear effects within the gain term S_{21} of an arbitrary 2-port network. In addition, the effect of output power saturation is also taken into account using a continuous function to ensure numerical convergence while preserving the architected non-linear behavior. It was also demonstrated how the core analysis can be extended to account for the complex impedance nature of the ports. A final comparison was conducted between results obtained from a transistor level LNA and the developed models. A general good agreement was observed.

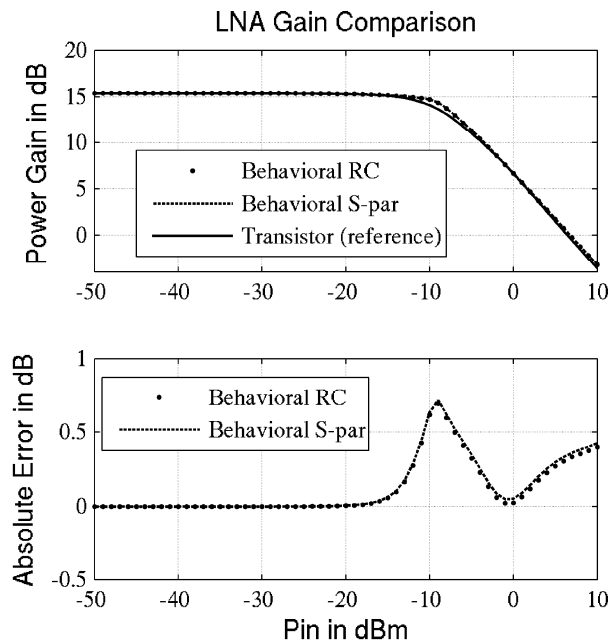

Figure 5: Comparison between behavioral and transistor level simulations in terms of power gain (top) and absolute error (bottom). Transistor level results are taken as the reference.

7. References

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[10] Questa ADMS™ User's Manual, release 2009.2.

8. Appendix A

```
-----------------------------------------------
library ieee;
  use ieee.electrical_systems.all;
library IEEE;
  use IEEE.MATH_REAL.all;
library mgc_ams;
  use mgc_ams.Eldo.all;

entity lna_sp is
    generic (
      s11      : real    := -30.0; --in dB
      s12      : real    := -35.0; --in dB
      s21      : real    :=  10.0; --in dB
      s22      : real    := -30.0; --in dB
      Z01      : real    :=  50.0; --in Ohms
      Z02      : real    :=  50.0; --in Ohms
      IIP2     : real    :=  3.0;  --in dBm
      IIP3     : real    :=  3.0;  --in dBm
      T_amb    : real    :=  27.0; --in Celsius
      NF       : real    :=  1.4); --in dB
    port (
      terminal ain       : electrical;
      terminal aout      : electrical);
end entity lna_sp;
-----------------------------------------------
architecture rf of lna_sp is
  terminal anoise    : electrical;
  constant real_IIP2 : real :=
                       10.0**((IIP2-30.0)/10.0);
  constant real_IIP3 : real :=
                      10.0**((IIP3-30.0)/10.0);
  constant real_s11  : real := 10.0**(s11/20.0);
  constant real_s12  : real := 10.0**(s12/20.0);
  constant real_s22  : real := 10.0**(s22/20.0);
  constant real_s21  : real := 10.0**(s21/20.0);
  constant Pmax      : real := IIP3 - 9.6;
  constant real_Pmax : real :=
                      10.0**((Pmax-30.0)/10.0);
  constant V1_max    : real :=
                      sqrt(2.0*Zo1*real_Pmax);
  quantity V1     across I1     through anoise;
  quantity V2     across I2     through aout;
  quantity Vnoise across anoise to ain;
  quantity V1_int    : real := 1.0;
  quantity V1_eff    : real := 1.0;
  quantity I1_eff    : real := 1.0;
  quantity a1        : real := 1.0;
  quantity a2        : real := 1.0;
  quantity b1        : real := 1.0;
  quantity b2        : real := 1.0;

  constant k2        : real :=
                -1*sqrt(1-s11_real**2))*real_s21/
                              sqrt(2.0*real_IIP2);
  constant k3        : real :=
            -(4.0/6.0)*(1-s11_real**2)*real_s21/
                                      real_IIP3;
  constant delta     : real := 1.0e-9;
  constant F         : real := 10.0**(NF/10.0);
  constant Ns        : real :=
             4.0*Zo1*1.381319e-23*(T_amb+273.0);
  constant Na        : real := Ns*(F-1.0);

 component ELDO_Noise_Src is
    generic (
      Na             : real := 1.0e-20);
    port (
      terminal anoise, ain : electrical);
  end component ELDO_Noise_Src;
attribute Eldo_device  of ELDO_Noise_Src :
   component is "ELDO_Noise_Source";
  attribute Eldo_file_name   of ELDO_Noise_Src :
   component is Eldo_subckt;
  attribute Eldo_subckt_name of ELDO_Noise_Src :
   component is "/run/Eldo_white_noise_vsrc.ckt";
begin  -- rf
  -- White noise source instantiation
  X_ELDO_Noise_Src :  ELDO_Noise_Src
    generic map (
      Na => Na)
    port map (
      anoise, ain );

  -- V1_eff calculation accounting for the
  -- saturation effect
  V1_int == -( -V1 - 0.5 * ( (-V1    -
     V1_max) + sqrt( (-V1    - V1_max)**2 +
     4.0*delta**2) ) );
  V1_eff == V1_int - 0.5 * ( (V1_int -
     V1_max) + sqrt( (V1_int - V1_max)**2 +
     4.0*delta**2) );

  -- Input Impedance Modeling
  V1     == I1 * Zo1 * (1.0+real_s11)/(1.0-
            real_s11);

  -- Input and output normalized waves definition
  a1 == 0.5 * (V1_eff/sqrt(Zo1) +
        I1_eff*sqrt(Zo1));
  a2 == 0.5 * (V2/sqrt(Zo2)    +
        I2*sqrt(Zo2));
  b1 ==  0.5 * (V1_eff/sqrt(Zo1) -
        I1_eff*sqrt(Zo1));
  b2 ==  0.5 * (V2/sqrt(Zo2)    -
        I2*sqrt(Zo2));

  -- S-parameters definition
  b1 == real_s11*a1 + real_s12*a2;
  b2 == real_s21*a1 + k2*a1**2 + k3*a1**3 +
        real_s22*a2;
end architecture rf;
-----------------------------------------------
```